Operator's Manual

CAN-Interface

Multi-Channel High Voltage Power Supply Module

Note

The information in this manual is subject to change without notice. We take no responsibility for any error in the document. We reserve the right to make changes in the product design without reservation and without notification to the users.

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1. General information

Each single HV channel is independently controllable. The EHS, EDS, NHS, MICC and MICP are prepared for mounting into a crate. The HPS devices are used standalone. The units are software controlled via CAN-Interface through a PC or similar controller.
We offer a comfortable control program “isegCANHVControl” for up to 64 iseg modules with CAN interface under Windows and „iseg OPC Control“ in connection with the „iseg OPC Server”.

Using the w-ie-ner Mpod crate it is possible to control up to 10 modules via Ethernet-SNMP Interface.

2. General settings and options

Please note that there are additional hardware features for these devices in this manual called **OPTION**. The use of an access without the hardware implementation will be described under **OPTION** in manual.

Devices with different settings of bit rate do not work on the same bus.

The permanent storage of a write access exists only if it is described as mode in the manual.

The refresh of actual channel values is made in each program cycle of the module – approximately every 10ms x number of channels?.

The refresh of actual values of module is made in each 2nd program cycle – approximately every 20ms x number of channels?

The refresh of actual board temperature value is made approximately every 5 up to10 s.

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3. Operation principals

3.1 Remote interface control

The Multi-Channel HV modules are controlled via a remote interface. The communication between an application and the module is performed by the transmission of data items. A data item is a unit to be submitted to and/or received from the module. It can represent a specific quantity or a union of single bits. The majority of the data items are standard for all Multi-Channel HV modules and are described in the interface manual in detail. Data items for optional functions are described in the interface options manual.

A general distinction can be made between data items to control individual HV channels and data items to control the HV modules with the sum of all contained channels.

The former group includes the following data items, which exist for every single HV channel:

- items to handle channel status, control and event's
- items to set the voltage or current, bounds, interlock maximum and minimum
- items to read the measured voltage and current
- items to read the nominal voltage and current

The following data items control the properties of the whole HV module. These items exist only once per module:

- items to handle module status, control and event's
- voltage ramp speed (is the same for all HV channels)
- current ramp speed (is the same for all HV channels)
- restart time after recalling set values
- maximum set voltage
- maximum set current
- ADC samples per second
- digital filter setting

- power supply voltages
- temperature
- maximum voltage
- maximum current

3.1.1 Operation modes

There are three operation modes depending on the HV hardware and the module configuration.

3.1.2 Voltage control(CV)

In the mode Voltage control the module works as a constant voltage source. For this mode it is required that the value for current set (Iset) or current trip (Itrip) is greater than the resulting output current.

3.1.3 Current control(CC)

In the mode Current control the module works as a constant current source. For this mode it is required that the HV channel has implemented a current control and that the current set value Iset is smaller than the current that would result from set voltage and the load at the HV output.

3.1.4 Current trip

This is a special case of the voltage regulation. The module usually provides a constant output voltage, where the value of the parameter Itrip defines a current limit. If this value is reached or exceeded (e.g. by arcs), in this mode the channel will be switched off immediately.

3.1.5 Function KillEnable

KillEnable is a global control signal that defines the behaviour of the module if a given voltage (Vmax) or current limit (Imax/Iset/Itrip) is exceeded.

If **KillEnable is active** the violation of one of the limits will trigger a Kill-signal in the respective channel. This signal will switch off the channel immediately without ramp.

If **KillEnable is inactive** and one of the limits Imax/Iset or Itrip is exceeded the following will happen:

HV hardware with current control - switch the channel from voltage control into current control.

HV hardware without current control – a trip in the channel hardware will switch off the high voltage generation. Then the module automatically starts to restore the HV via a voltage ramp to the set voltage. If the HV is held during the trip, e.g. by an external capacity load, the recovery of the HV starts from the voltage at the output. The auto-recovery of the voltage is performed only once in a time span of 10 minutes. If the channel trips a second time within the 10 minutes the HV will be switched off.

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3.1.6 Additional current measuring range (Option)

Some modules can be equipped with a second current measuring range to capture small current values. The range is automatically detected. In the second range the values will be converted with a higher resolution. The value is in the same floating point format as in the first range. The device control protocol allows to request which range is active.

Important information, the second range cannot be activated if:
- function KillEnable is on.
- delayed trip function is switched on.
- a voltage ramp is running.
- the module operates in CC mode.

3.2 Control and Status items

3.2.1 Controls

Control items encapsulate a number of bits which allow to switch On or Off specific functions. There is a control item for the module (**ModuleControl**) and one for each channel (**ChannelControl**). Control bits that are used to switch a function permanently are named “set...” (e.g. “setON” to switch a channel On of Off). Bits that initiate the execution of a task just once are named “do...” (e.g. “doClear” to clear all events).

3.2.2 Status and events

Status items contain a register that encapsulates bits that indicate the current status of the module or channel. Status bits are named starting with “is...”. The status always displays only present conditions, if a condition has changed corresponding status bits will be updated.
Unlike the status, event items record previous conditions (e.g. exceeded limits, trips etc.). If an event is registered the corresponding event bit is set permanently to “1” and will keep the information until explicitly reset. Event bits are named starting with “E...”.

status	Summary of actual condition of module, channel or group
event	Event, that characterizes a former or actual special condition of module, channel or group

3.2.3 Event status and event mask

To avoid the need for checking all event sources permanently for incoming events, the module provides a hierarchical chain for the combination of the events to a single status bit. The structure for the event processing allows a combination of events coming from the module status, the status of the channels and the group status. For each event status item a corresponding event mask item is provided. The event mask defines which event status bits contribute to the combined event status.

Event status	Events that have been registered so far
Event mask	Filter to define which individual events contribute to the summarized event

Between event status items and the corresponding mask is a bit by bit correspondence. The bits in the mask are named starting with “ME...”. If the mask bit is set, the occurring of the respective event will activate the combined event. In turn these sum events are collected in an event status register and connected with an event mask register at this higher level.

If an event bit in the EventStatus is active and the corresponding bit in the EventMask is set, it is not possible to ramp up the voltage or to activate the HV generation if it has been switched off. To unblock this the EventStatus bits must be reset by writing “1” on the corresponding bit positions.

Individual events in the channel event status are starting point of the event combination logic.
First each event status bit for the channel is combined with the corresponding bit in the event mask using a logical AND. Then an event status bit for the channel is generated by combining all resulting bits with a logical OR. The full logical operation is given by

```
EventChannelStatus[n] =  (Channel[n].EventVoltageLimit AND Channel[n].MaskEventVoltageLimit) OR
                         (Channel[n].EventCurrentLimit AND Channel[n].MaskEventCurrentLimit) OR
                         (Channel[n].EventCurrentTrip AND Channel[n].MaskEventCurrentTrip) OR
                         (Channel[n].EventExtInhibit AND Channel[n].MaskEventExtInhibit) OR
                         (Channel[n].EventVoltageBounds AND Channel[n].MaskEventVoltageBounds) OR
                         (Channel[n].EventCurrentBounds AND Channel[n].MaskEventCurrentBounds) OR
                         (Channel[n].EventControlledVoltage AND Channel[n].MaskEventControlledVoltage) OR
                         (Channel[n].EventControlledCurrent AND Channel[n].MaskEventControlledCurrent) OR
                         (Channel[n].EventEmergency AND Channel[n].MaskEventEmergency) OR
                         (Channel[n].EventEndOfRamp AND Channel[n].MaskEventEndOfRamp) OR
                         (Channel[n].EventOnToOff AND Channel[n].MaskEventOnToOff ) OR
                         (Channel[n].EventInputError AND Channel[n].MaskEventInputError)
```

The result of the first step for all channels is stored in the register EventChannelStatus.
In the next step all bits of the EventChannelStatus are combined to a single status bit, using the corresponding mask (EventChannelMask). The logical operation is given by

```
EventChannelActive =     (EventChannelStatus[0] AND EventChannelMask[0]) OR
                         (EventChannelStatus[1] AND EventChannelMask[1]) OR
                         ...
                         (EventChannelStatus[n] AND EventChannelMask[n])
```

A second branch in the event processing logic treats events generated by the status of the module. The following scheme applies to these module events:

```
EventModuleActive =      (EventTemperatureNotGood AND MaskEventTemperatureNotGood) OR
                         (EventSupplyNotGood AND MaskEventSupplyNotGood) OR
                         (EventSafetyLoopNotGood AND MaskEventSafetyLoopNotGood)
```

A third branch combines events generated by groups (monitor group, timeout group, see chapter 3) Group events are stored in the status register EventGroupStatus. The mask EventGroupMask is used to generate the combined bit EventGroupActive with the following operation:

```
EventGroupActive =       (EventGroupStatus[0] AND EventGroupMask[0]) OR
                         (EventGroupStatus[1] AND EventGroupMask[1]) OR
                         ...
                         (EventGroupStatus[32] AND EventGroupMask[32])
```

Finally the three branches are combined to the bit IsEventActive in the register ModuleStatus:

```
IsEventActive =          EventChannelActive OR EventModuleActive OR EventGroupActive
```


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3.3 Summarizing channel characteristics into groups

The module provides a highly flexible group functionality. A group is a combination of all or a selection of channels with the ability to control or monitor a specified quantity or characteristic of all included channels. There are two classes of groups “Fix Groups” and “Variable Groups”. The former are predefined groups that allow to set single specification values in all channels. The latter are configurable groups that allow to customize the logical structure of the module to the logical structure of the application. They allow an arbitrary assignment of channels and provide a wide range of functionality, structured in four predefined group types. Up to 32 Variable Groups can be defined. The predefined group types are:

3.3.1 Set Group

- sets a specified channel characteristic in all selected channels
- no event generation

3.3.2 Status Group

- represents the status (condition) of a channel characteristic for all channels
- no event generation

3.3.3 Monitor Group

- monitors the condition of a channel characteristic for selected channels
- event generation when the condition changes
- configurable response (e.g. switch off)

3.3.4 Timeout Group

- monitors the current trip in selected channels
- to employ this group the signal KillEnable must be turned off
- Event generation only after expiry of a predefined time within which the trip condition must be active
- configurable response (e.g. switch off)

3.3.5 Responses on events (Soft-Kill features)

Event generating groups can be configured to perform one out of four predefined responses if the event has been generated:

- shut down of the whole module without ramp
  - high voltage in all channels of the module is switched off
- switch off all channels that are members of the group without ramp
  - high voltage in all channels of the group is switched off
- switch off all channels that are members of the group with ramp
  - high voltage in all channels of the group is ramped down
- no response
  - no change

4. Communication via Interface

All modules are controlled via a serial CAN bus interface according to CAN bus specification 2.0A. The actual control protocol is the "Enhanced Device Control Protocol" and is explained more precisely in the following sections.
Furthermore it is implemented a second command set, which corresponds to the older standard protocol "Device Control Protocol". The description of the Device Control Protocol is carried out in the corresponding manual.

4.1 Enhanced Device Control Protocol EDCP

The communication between the controller and the module is working according to the Enhanced Device Control Protocol EDCP, which has been designed for instruments of Multi-Channel systems by iseg Spezialelektronik GmbH. This protocol is working according to the master slave principle. Therefore, the control of the HV device through a controller in the superior layer is the master in this system, while the module (as a Front-end device with intelligence) is the slave.
The data exchange between the controller and the HV device is working with help of data frames. These data frames are made out of one direction bit DATA_DIR, one 16bit DATA_ID and further data bytes. The direction bit DATA_DIR defines whether the data frame is a write or read-write access. Write access means that the host writes data into the module, read-write access means that the host wants to read data from the module (this is the read access), and the module answers by a write access.

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The DATA_ID is characterized through the first bit of the data frame with DATA_ID.b15=0 of EDCP frames (DATA_ID.bit7=1 of standard DCP frames). In order to code the type of an access the bit14=1 for a single channel access (symbol S), b13=1 for a group access (symbol G) and b12=1 for a module access (symbol M).

The next tables will give an overview of the parts of the EDCP:

Access	**DATA DIR**	**DATA_ID bits**																**CHN bits**							
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Enhanced DATA_ID	**1/0**	**0**	**S**	**G**	**M**	x	x	x	x	x	x	x	x	x	x	x	x								
Single channel **CHN** **Write access**	**0**	0	1	0	0	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0	C7	**CHN** (0 to 255)						C0
Single channel **CHN** **Read-write access**	**1/0**	0	1	0	0	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0	C7	**CHN** (0 to 255)						C0
Module **Write access**	**0**	0	0	0	1	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0								
Module **Read-write access**	**1/0**	0	0	0	1	M11	G10	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0								

If the type of the data frame is a single channel access it will code the corresponding channel information with help of the next multiplex of channel byte (symbol **CHN**). If the type of the data frame is a module access then a DATA_ID is necessary only.

Access	**DATADIR**	**DATA_ID bits**																**CHN / MBR bits**								
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	
Enhanced DATA_ID	**1/0**	**0**	**S**	**G**	**M**	x	x	x	x	x	x	x	x	x	x	x	x									
Single channel **CHN** of members **MBR** **Read-write access**	**1** **0**	0	1	1	0	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0	M15	**MBR**						M0	**OFFSET**
																		C7	**CHN**						C0	0, 16, 32,

If the type of the data frame is a single channel and group access then it will code the corresponding channel members with help of the next 16bit word (symbol **MBR,** channel15=bit15, .. , channel0=bit0) followed by an **OFFSET** byte to have a channel start index in steps of 16. If a HV device has received such a message it will transmit the information of the channels which are members in a very expeditious mean.

Access	**DATADIR**	**DATA_ID bits**									**NBR / CHN bits**								
		15	14	13	12	11	10	…	1	0	7	...	0						
Group of members **MBR** **Write access**	**0**	**0**	**S**	**G**	**M**	x	x	…	x	x	N7	**NBR**	N0	**OFFSET**	M15	**MBR**	M0	**Type**	
Group of members **MBR** **Read-write access**	**1** **0**	0	0	1	0	G11	G10	...	G1	G0	C7	**CHN**	C0	0, 16, 32	M15	**MBR**	M0		
											C7	**CHN**	C0						

If the type of the data frame is a group access than it will coded the corresponding group number symbol **NBR**, the channel members symbol **MBR** and the channel start index symbol **OFFSET**.

These data frames correspond to a transfer into layer 3 (Network Layer) and layer 4 (Transport Layer) of the OSI model of ISO. The transmission medium is the CAN Bus according to specification 2.0A, related to level1 (Physical Layer) and level 2 (Data Link Layer).

The Enhanced Device Control Protocol EDCP has been matched to the CAN Bus according to specification CAN 2.0A. Therefore specials of layer 1 and 2 are mentioned only if absolutely necessary and if misunderstandings of functions between the Transport Layer and functions of the Data Link Layer may be possible. The communication between the controller and a module on the same bus segment can be described as follows.

4.2 CAN-Bus Implementation

The data frame structure is matched to the message frame of the standard-format according to CAN specification 2.0A, whereas looking from the point of view of the CAN protocol a pure data transmission will be done, which is not applying to the protocol.

The data frame of the EDCP will be transferred as data word with n bytes length in the data field of the CAN frame according to the specific demand of the related access. Therefore this results into a Data Length Code (DLC) of the CAN-protocol of n.

It is possible to transfer 8 data bytes that apply to the DLC field with decreasing values.

The addressing of the Front-end device is also made using the 11 bit identifier of the CAN protocol.

In order to keep the CAN segment open also for other protocols, the address room has been limited to 64 nodes.

ID10 is dominant.

ID9 When the Event structure of the module was configured and the bit isEvntActive in the ModuleStatus was triggered, then the module will send the DCP Module frame General status as an active message with higher priority (ID9 = 0) than normal messages.

ID8 to ID3
allow the addressing of 64 Front-end devices (ID3: A0 = 2^0 ;...; ID8: A5 = 2^5), see *3.2 Back Panel* also.

ID2 is used for a special network management service (NMT).

ID1 is not used.

ID0 is used for defining the direction of the data transfer (DATA_DIR). The controller therefore will start a read-write access for data with DATA_DIR = 1 and will send data with DATA_DIR=0. The Front-end device responds to the data request by sending the corresponding data with DATA_DIR = 0.

That means all “even” CAN-ports (Identifier) are interpreted as ‘Write ports’ all “odd” CAN ports as ‘ Read ports’.
Only if the Front-end device is not registered at the controller or if it does not receive valid data during a longer time period (ca. 1 min), then it will actively send the registration frame with DATA_DIR = 1 (see also item 4.3). The RTR Bit is always set to zero.
In one CAN segment modules with unequal identifier and equal bit rate are allowed only. The factory fixed bit rate is written on the sticker of the 96-pin connector.

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Data formats:

The data format on the network is big endian, i.e. on Intel computers, the value is stored byte-wise reverse. To convert floating-point values to their hexadecimal representation, the online calculator http://babbage.cs.qc.edu/IEEE-754/ can be used.

UI1	unsigned character
SI1	signed character
UI2	unsigned short integer (16 bit)
UI3	unsigned integer (24 bit)
UI4	unsigned integer (32 bit)
R4	float according to IEEE-754 single precision format

Example Vset = 1000 V:

Data-Bytes on the network – 0x44 0x7a 0x00 0x00
Data-Bytes in computers using a little endian memory – 0x00 0x00 0x7a 0x44

Conventional CAN data frame to control of the HV modules, see ehq_multi_channel_can also.

S	Identifier	R			DLC	n – data bytes (1 to 8)					CRC	ack
O		T	0	0	(n=1-8)	DATA_ID Single channel access	CHN	DATA_(n-3)□ 0	DATA_(n-4)≥ 0	DATA_ ...		F.
F	b10 … b0	R	Reserve		b3 … b0	b15=0 1 0 0 … b0	C7 … C0	b7 … b0	b7 … b0	b7 … b0	15 bit	

S	Identifier	R			DLC	n – data bytes (1 to 8)					CRC	ack
O		T	0	0	(n=1-8)	DATA_ID Multiple single channels access	MBR	DATA_(n-4)□ 0	DATA_(n-5)≥ 0	DATA_ ...		F.
F	b10 … b0=1	R	Reserve		b3 … b0	b15=0 1 1 0 … b0	M15 … M0	b7 … b0	b7 … b0	b7 … b0	15 bit	

S	Identifier	R			DLC	n – data bytes (1 to 8)					CRC	ack
O		T	0	0	(n=1-8)	DATA_ID Group access	NBR	OFFSET	ChList	Type ...		F.
F	b10 … b0	R	Reserve		b3 … b0	b15=0 0 1 0 … b0	N7 … N0	b7 … b0	b15 … b0	b15 … b0	15 bit	

S	Identifier	R			DLC	n – data bytes (1 to 8)				CRC	ack
O		T	0	0	(n=1-8)	DATA_ID Module access	DATA_(n-2)□ 0	DATA_(n-3)□ 0	DATA_ ...		F
F	b10 … b0	R	Reserve		b3 … b0	b15=0 0 0 1 … b0	b7 … b0	b7 … b0	b7 … b0	15bit	

ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
0	0	0	0	0	0	0	0	1	0	DATA_DIR

1. Acceptance-Filter of the CAN-Controller is set to NMT service identifier

ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
0	P	A5	A4	A3	A2	A1	A0	0	0	DATA_DIR

2. Acceptance-Filter of the CAN-Controller is set to FE-address A0 - A5

The Front-end device must do:

- Processing of NMT services via broadcast messages inside of the CAN segment
- Processing of the single accesses with direct channel values.
- Processing of group information of the module.
- Self-registration in the higher level through sending the module address.
- Building of status information.
- Send an active error message with higher priority if one of the bits - sum status, supply voltages or safety loop - in the group access “General status module” not has been set (the module must be configured as a CAN-node with an Active-CAN message function).

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4.3 Summary of CAN data frame accesses via the NMT service identifier

Access	DATA_DIR	NMT DATA_ID Bit								read / write / active	DATA-Bytes	Page
	ID0	7	6	5	4	3	2	1	0			
No NMT DATA_ID	x	**0**	x	x	x	x	x	x	x			
NMT service CAN segment:	**0**	**1**	**1**	**N3**	**N2**	**N1**	**N0**	**R1**	**R0**			
NMT Address (MICC only)	0/1	0	0	1	1	0	0	0	0	w	0/2/3	
NMT Start	0	1	1	0	0	0	1	x	x	w	1	18
NMT Stop	0	1	1	0	0	1	0	x	x	w	1	18
NMT Reset CAN	0	1	1	0	0	1	1	x	x	w	1	18
NMT Reset hardware	0	1	1	0	1	0	0	x	x	w	1	18
NMT set of Bit rate	0	1	1	0	1	0	1	x	x	w	3	18
NMT temperature set	0	1	1	0	1	1	0	x	x	w	3	19
NMT mode set	0	1	1	1	0	0	0	x	x	w	2/6	19
NMT set standard DCP or enhanced DCP	0	1	1	1	0	0	1	x	x	w	2	19
NMT channel group set	0	1	1	1	0	1	0	x	x	w	8/6	19
NMT module set	0	1	1	1	0	1	1	x	x	w	8/6	19
N_i: NMT access												
R_i: reserved												

NMT Address (MICC only)

Access	CAN ID (NMT)	RTR	EXT_INSTR	DATA_DIR	DATA_ID	DATA_1	DATA_0
NMT-RTR master	0x004	1	0	0	-	-	-
NMT-RTR board reply	0x003	0	0	0	0xC0	address	-
NMT Addess master write	0x004	0	0	0	0xC0	old address	new address

NMT Start — The state of all Front-end devices is going to OPERATIONAL (see Appendix C)

NMT Stop — The state of all Front-end devices is going to PREPARED
This is necessary before storing any information permanently in EEPROM or execute one of the following NMT services

NMT Reset CAN — re - initialise all connected iseg Multi-Channel CAN devices.

NMT Reset hardware — execute a hardware reset of all connected CAN devices.

NMT set of Bit rate — set a new bit rate for all connected iseg Multi-Channel CAN devices

(DATA_1 / DATA_0 see group access Bit rate)

NMT set of temperature — An offset for the calculation of the temperature will be calculated in all modules which receive this message.

all devices

DATA_1 to DATA_0 — measured temperature in tenth parts of °C
UI2

DATA_1	DATA_0
MSB	LSB

NMT mode

Mode	Data_0	Description
NORMAL_MODE	000	Operating Mode “Operational" without any condition
FACTORY MODES	001 - 005	will used in production of the modules only!
LIVE_INSERTION_MODE	006	Mode to avoid events during a live insertion

NMT set standard DCP or enhanced DCP: DATA_0=0 standard DCP DCP
DATA_0=1 enhanced DCP EDCP

NMT broadcast messages

NMT channel group set frame:

Access	DATA_DIR	NMT DATA_ID	GROUP	EDCP DATA_IDEDCP Multiple Single Channels Access	DATAn	DATAn-1	DATAn-2	DATAn-3
NMT group voltage set	0	0xe8	Group	0x6100	Voltage [R4] ↥			
NMT group current set	0	0xe8	Group	0x6101	Current [R4] ↥			
NMT group control set	0	0xe8	Group	0x6001	Control [UI2] ↥			
NMT group event mask set	0	0xe8	Group	0x6003	Event mask [UI2] ↥			

Group 0..255 (group = 0 after power on of the module)

NMT module set frame:

NMT voltage ramp speed set	0	0xec	xx	0x1100	Voltage ramp speed [R4] ↥	
NMT current ramp speed set	0	0xec	xx	0x1101	Current ramp speed [R4] ↥	
NMT control set	0	0xec	xx	0x1001	Control [UI2] ↥	
NMT event mask	0	0xec	xx	0x1003	Event mask [UI2] ↥	
NMT event channel mask	0	0xec	xx	0x1005	Event mask [UI2] ↥	

xx reserved

With one of the **NMT channel group set** or the **NMT module set** frames a message is sent to the corresponding data point of the table above in kind of a broadcast information for all channels, which have the same group number **GROUP**. The detailed description of the frames can be found by a click on the arrows of the tables. The EDCP Single Channel Access **GroupNumber** (described on page 30) handles the distribution of a group number for each channel.

The **NMT channel group set** and **NMT module set** frames has been implemented since following firmware releases:

Name of firmware	Firmware release	Device class
E16D0	00.04.02.01	21
E16D1	00.04.02.01	21
E08C0	00.02.02.00	24
E16C1	00.01.00.00	70
E08C2	00.01.00.00	27
E08F0	00.02.02.08	25
E08F2	00.04.00.06	26

Example: Switch ON all channels of the whole system (group number after reset of all channels is zero)

ID	DLC	NMT DATA_ID	GROUP	EDCP DATA_ID Multiple Single Channel Access	Channel control
0x004	0x6	0xe6	0x00	0x6001	0x0008

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4.4 Summary of CAN data frame accesses via the Front-end-address identifier

Multi-channel High Voltage CAN modules are made out of one or two PCBs (in order to double the number of HV channels) and one digital CAN Interface per PCB.
Each module board has to be controlled separately via its own CAN nodes identifier (see chapter above).

4.4.1 List to access of the EDCP made for HV boards up to 255 channels

4.4.1.1 EDCP Single Channel Accesses

Access	DATA_DIR	DATA_ID																read / write / active	DATA-Bytes	Page
		Word	Bit																	
	ID0	hex	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
DATA_ID			**0**	**S**	**G**	**M**	x	x	x	x	x	x	x	x	x	x	x	x			
Single channel access	**1/0**	**0x4xxx**	**0**	**1**	**0**	**0**	**S11**	**S10**	**S9**	**S8**	**S7**	**S6**	**S5**	**S4**	**S3**	**S2**	**S1**	**S0**			
ChannelStatus	1	0x4000	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	r	3/5	25
ChannelControl	0/1	0x4001	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	w/r	3/5	26
ChannelEventStatus	1/0	0x4002	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	r/w	3/5	26
ChannelEventMask	0/1	0x4003	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	w/r	3/5	27
DelayedTripAction	0/1	0x4005	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1	w/r	3/4	28
DelayedTripTime	0/1	0x4006	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	w/r	3/5	28
ExternalInhibitAction	0/1	0x4007	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	w/r	3/4	28
VoltageSet	0/1	0x4100	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	w/r	3/7	29
CurrentSet / CurrentTrip	0/1	0x4101	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	1	w/r	3/7	29
VoltageMeasure	1	0x4102	0	1	0	0	0	0	0	1	0	0	0	0	0	0	1	0	r	3/7	30
CurrentMeasure	1	0x4103	0	1	0	0	0	0	0	1	0	0	0	0	0	0	1	1	r	3/7	30
VoltageBounds	0/1	0x4104	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	w/r	3/7	30
CurrentBounds	0/1	0x4105	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0	1	w/r	3/7	30
VoltageNominal	1	0x4106	0	1	0	0	0	0	0	1	0	0	0	0	0	1	1	0	r	3/7	31
CurrentNominal	1	0x4107	0	1	0	0	0	0	0	1	0	0	0	0	0	1	1	1	r	3/7	31
CurrentMeasure Range	1	0x4109	0	1	0	0	0	0	0	1	0	0	0	0	1	0	0	1	r	3/8	31
VctCoefficient	1/0	0x4120	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	r/w	3/7	31
TemperatureExternal	1/0	0x4121	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	1	r/w	3/7	31
GroupNumber	1/0	0x4200	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	w/r	3/4	32

S DATA_ID type bit for a EDCP-frame of an access to a single channel
G DATA_ID type bit for a EDCP-frame of an access to a group of channels
M DATA_ID type bit for a EDCP-frame of an access to the whole module
$S_{i:(i=0..11)}$ single channel access bits

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4.4.1.2 EDCP Multiple Single Channels Access

Access	DATA_DIR	DATA_ID Word	DATA_ID Bit																read / write / active	DATA-Bytes	Page
	ID0	hex	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
DATA_ID			**0**	**S**	**G**	**M**	x	x	x	x	x	x	x	x	x	x	x	x			
Single channel access	**1**	**0x6xxx**	**0**	**1**	**1**	**0**	**S11**	**S10**	**S9**	**S8**	**S7**	**S6**	**S5**	**S4**	**S3**	**S2**	**S1**	**S0**			
ChannelStatus	1	0x6000	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	r	5/5	25
ChannelControl	1	0x6001	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	r	5/5	26
ChannelEventStatus	1	0x6002	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	r	5/5	26
ChannelEventMask	1	0x6003	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	r	5/5	27
DelayedTripAction	0/1	0x6005	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	w/r	3/4	28
DelayedTripTime	0/1	0x6006	0	1	1	0	0	0	0	0	0	0	0	0	0	1	1	0	w/r	3/5	28
ExternalInhibitAction	0/1	0x6007	0	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	w/r	3/4	28
VoltageSet	1	0x6100	0	1	1	0	0	0	0	1	0	0	0	0	0	0	1	0	r	5/7	29
CurrentSet / CurrentTrip	1	0x6101	0	1	1	0	0	0	0	1	0	0	0	0	0	0	1	1	r	5/7	29
VoltageMeasure	1	0x6102	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	r	5/7	30
CurrentMeasure	1	0x6103	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	1	r	5/7	30
VoltageBounds	1	0x6104	0	1	1	0	0	0	0	1	0	0	0	0	0	1	0	0	r	5/7	30
CurrentBounds	1	0x6105	0	1	1	0	0	0	0	1	0	0	0	0	0	1	0	1	r	5/7	30
VoltageNominal	1	0x6106	0	1	1	0	0	0	0	1	0	0	0	0	0	1	1	0	r	5/7	31
CurrentNominal	1	0x6107	0	1	1	0	0	0	0	1	0	0	0	0	0	1	1	1	r	5/7	31
CurrentMeasure Range	1	0x6109	0	1	1	0	0	0	0	1	0	0	0	0	1	0	0	1	r	3/8	31
VctCoefficient	1/0	0x6120	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	r/w	3/7	31
TemperatureExternal	1/0	0x6121	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	1	r/w	3/7	31
ChannelGroup	0	0x6200	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	w	6	32

S DATA_ID type bit for a EDCP-frame of an access to single channel
G DATA_ID type bit for a EDCP-frame of an access to a group of channels
M DATA_ID type bit for a EDCP-frame of an access to the whole module
$S_{i:(i=0..11)}$ single channel access bits

4.4.1.3 EDCP Module Access

Access	DATA_DIR	DATA_ID																	read / write / active	DATA-Bytes	Page
		Word	Bit																		
	ID0	hex	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
DATA_ID			**0**	**S**	**G**	**M**	x	x	x	x	x	x	x	x	x	x	x	x			
Module access	**1/0**	**0x1xxx**	**0**	**0**	**0**	**1**	**M11**	**M10**	**M9**	**M8**	**M7**	**M6**	**M5**	**M4**	**M3**	**M2**	**M1**	**M0**			
ModuleStatus	1	0x1000	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	r	2/4	34
ModuleControl	0	0x1001	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	w/r	4/2	35
ModuleEventStatus	1/0	0x1002	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	r/w	2/4	35
ModuleEventMask	0/1	0x1003	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	w/r	4/2	36
ModuleEventChannelStatus	1/0	0x1004	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	r/w	2/4	36
ModuleEventChannelMask	0/1	0x1005	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	1	w/r	4/2	36
ModuleEventGroupStatus	0/1	0x1006	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1	0	r/w	2/4	37
ModuleEventGroupMask	0/1	0x1007	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1	1	w/r	4/2	38
VoltageRampSpeed	0/1	0x1100	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	w/r	6/2	38
CurrentRampSpeed	0/1	0x1101	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1	w/r	6/2	38
VoltageMax	r	0x1102	0	0	0	1	0	0	0	1	0	0	0	0	0	0	1	0	r	2/6	39
CurrentMax	r	0x1103	0	0	0	1	0	0	0	1	0	0	0	0	0	0	1	1	r	2/6	39
Supply24	r	0x1104	0	0	0	1	0	0	0	1	0	0	0	0	0	1	0	0	r	2/6	40
Supply5	r	0x1105	0	0	0	1	0	0	0	1	0	0	0	0	0	1	0	1	r	2/6	40
BoardTemperature	0/1	0x1106	0	0	0	1	0	0	0	1	0	0	0	0	0	1	1	0	r	2/6	40
ThresholdArmErrorDetection	0/1	0x1107	0	0	0	1	0	0	0	1	0	0	0	0	0	1	1	1	w/r	6/2	40
SerialNumber	1	0x1200	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	1	r	2/6	41
FirmwareRelease	1	0x1201	0	0	0	1	0	0	1	0	0	0	0	0	0	0	1	0	r	2/6	41
BitRate	0/1	0x1202	0	0	0	1	0	0	1	0	0	0	0	0	0	0	1	0	r	4/2	41
NameOfFirmware	1	0x1203	0	0	0	1	0	0	1	0	0	0	0	0	0	0	1	1	r	5/6	36
ADC SamplesPerSecond	0/1	0x1204	0	0	0	1	0	0	1	0	0	0	0	0	0	1	0	0	w/r	4/2	37
DigitalFilter	0/1	0x1205	0	0	0	1	0	0	1	0	0	0	0	0	0	1	0	0	w/r	4/2	37

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ModuleOption	1	0x1280	0	0	0	1	0	0	1	0	1	0	0	0	0	0	0	0	r	6	38
ModuleOptionSpec	1	0x1290	0	0	0	1	0	0	1	0	1	0	0	1	0	0	0	0	r	7	38
ModuleCommMode	1	0x12a0	0	0	0	1	0	0	1	0	1	0	1	0	0	0	0	0	w	4	38
Factory settings	1/0	0x140x	0	0	0	1	0	1	0	0	0	0	0	0	0	0	x	x	r/w	4/8	-

S	DATA_ID type bit for a EDCP-frame of an access to a single channel
G	DATA_ID type bit for a EDCP-frame of an access to a group of channels
M	DATA_ID type bit for a EDCP-frame of an access to the whole module
$M_{i:(i=0..11)}$	module access bits

4.4.1.4 EDCP Group Accesses

Access	DATA_DIR	DATA_ID																	read / write / active	DATA-Bytes	Page
		Word	Bit																		
	ID0	hex	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
DATA_ID			**0**	**S**	**G**	**M**	G11	G10	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0			
Groups SetGroup StatusGroup MonitorGroup TripGroup	**0/1**	**0x2000**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**w/r**	**8/4**	**44**
VoltageSetAllChannels	**0**	**0x2100**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**w**	**6**	**49**
CurrentSetAllChannels	**0**	**0x2101**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**w**	**6**	**49**
SetOnOffAllChs		**0x2200**																	**r/w**	**6**	**44**
SetEmergencyAllChs		**0x2201**																	**r/w**	**6**	**45**
EventStatusVLimtAllChs		**0x2202**																	**r/w**	**6**	**45**
EventStatusCLimtAllChs		**0x2203**																	**r/w**	**6**	**46**
EventStatusTrpAllChs		**0x2204**																	**r/w**	**6**	**47**
EventStatusInhAllChs		**0x2205**																	**r/w**	**6**	**47**
SetOnOffChsExtender		**0x2280**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**r/w**	**6**	**48**
SetEmergencyChsExtender		**0x2290**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**1**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**r/w**	**6**	**48**

S DATA_ID type bit for a EDCP-frame of an access to a single channel
G DATA_ID type bit for a EDCP-frame of an access to a group of channels
M DATA_ID type bit for a EDCP-frame of an access to the whole module
$G_{i:(i=0..11)}$ group access bits

4.4.1.5 Important DCP Module Access

Access	EXT_INSTR	DATA_DIR	DATA_ID									read / write / active	DATA-Bytes	Page
			Byte	Bit										
	ID1	ID0		7	6	5	4	3	2	1	0			
Group access MODULE:	**0**	**1/0**		**1**	**1**	**M3**	**M2**	**M1**	**M0**	**R1**	**R0**			
GeneralStatus	0	1/0	0xc0	1	1	0	0	0	0	0	0	a	3	54
LogOnOff Front-end at the superior layer	0	1/0	0xD8	1	1	0	1	1	0	0	0	a/w	3	55

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4.5 Description of data information per DATA_ID in EDCP

4.5.1 EDCP Single Access

The single access describes the control of the channel properties. The range of the single access contains the accesses to the analog digital data items, to the status and the control words of the channels.

4.5.1.1 Channel status (single/multiple single read-write access)

EDCP frame: OPC SNMP ↑

Access	DATA_DIR	DATA_ID	CHN	DATA_1	DATA_0
master single read-	1	0x4000	M_x		
master single MBR read-	1	0x6000	Member		Offset
HV board write access	0	0x4000/0x6000	M_x	ChannelStatus	

Mx	Channel	0 ... 255
Member	Members	1 … 16
Offset	Channel member offset	0, 16, 32 … too access up to 255 channels
ChannelStatus	DATA_0 to DATA_1	UI2

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
isVLIM	isCLIM	isTRP	isEINH	isVBND	isCBND	isArcErr	isLCR	isCV	isCC	isEMCY	isRAMP	isON	IERR	isArc	res

The ChannelStatus register describes the actual status. Depending on the status of the module the bits will be set or reset.

The bit InputError will be set if the given parameter is not plausible or it exceeds the module parameters (e.g. if the command Vset=4000V is given to a module with NominalVoltage=3000V). The bit InputError is not be set if the given values are temporarily not possible (e.g. Vset=2800 at a module with NominalVoltage=3000V, but HardwareLimitVoltage=2500V). A certain signature which kind of input error it is does not exists.

isVLIM	IsVoltageLimitExceeded	voltage limit set by V_{max} is exceeded
IsCLIM	IsCurrentLimitExceeded	current limit set by I_{max} is exceeded
isTRP	IsTripExceeded	Trip is set when Voltage or Current limit or Iset has been exceeded (when KillEnable=1)
isEINH	IsExternalInhibit	External Inhibit
isVBND	IsVoltageBoundsExceeded	Voltage out of bounds
isCBND	IsCurrentBoundsExceeded	Current out of bounds
isArcErr	IsArcError	maximum number of allowed arcs is exceeded, high voltage has been turned off
isLCR	IsLowCurrentRange	Low or small current range of the current measurement
isCV	IsControlledVoltage	Voltage control active (evaluation is guaranteed when no ramp is running)
isCC	IsControlledCurrent	Current control active (evaluation is guaranteed when no ramp is running)
isEMCY	IsEmergencyOff	Emergency off without ramp
isON	IsOn	On
isRAMP	IsRamping	Ramp is running
IERR	InputError	Input error
isArc	isArc or IsRegulationError	at least one electrical arc is active or faster error detection of the channel hardware is not in regulation (check it every 5ms)
res	reserved	

isVLIM=0 channel is ok
isVLIM=1 the hardware voltage limit is exceeded
isCLIM=0 channel is ok
isCLIM=1 the hardware current limit is exceeded
(to detect a hardware voltage or current limit error flag the firmware has to evaluate the channel voltage and current at first)
isTRP=0 channel is ok
isTRP=1 V_O is shut off to 0V without ramp because the channel has been tripped.
isEINH=0 channel is ok
isEINH=1 External Inhibit was scanned
isVBND=0 channel is ok
isVBND=1 |Vmeas-Vset| > Vbounds
isCBND=0 channel is ok
isCBND=1 |Imeas-Iset| > Ibounds (to detect a voltage or current out of bound flag the firmware has to ramp the channel voltage Vset at first)

isArcErr=0 no arc error
isArcErr=1 maximum number of allowed arcs is exceeded
isLCR=0 high or standard current range
isLCR=1 low current range of the current measurement
sCV=1 channel is in state of voltage control
isCC=1 channel is in state of current control
isEMCY=1 channel is in state of emergency off, VO has been shut off to 0V without ramp
isON=0 channel is off
isON=1 channel voltage follows the Vset value
isRAMP=0 no voltage is in change
isRAMP=1 voltage is in change with the stored ramp speed value
IERR=0 no input-error
IERR=1 incorrect message to control the channel
isARC=0 no arc active / normal error evaluation
isARC=1 at least one electrical arc is active / fast detection of a regulation error (**OPTION**)

4.5.1.2 Channel control: (single write- and single/ multiple single read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	CHN	DATA_1	DATA_0
master write access	0	0x4001	M_x	ChannelControl	
master read-	1	0x4001	M_x		
master single MBR read-	1	0x6001	Member		Offset
HV board write access	0	0x4001/0x6001	M_x	ChannelControl	

Mx	Channel	0 ... 255
Member	Members	1 … 16
Offset	Channel member offset	0, 16, 32 … to access up to 255 channels
ChannelControl	DATA_0 to DATA_1	UI2

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
res	res	res	res	res	res	res	res	res	res	setEMCY	res	setON	res	res	res

The signals SetOn and SetEmergencyOff control are basic functions of the channel. The signal SetOn is switching ON the HV of the channel and is a precondition for giving voltage to the output. As far as a VoltageSet has been set and no event has occurred and is not registered yet (in minimum, bit 5 and bit 10 to 15 of the register Channel Event Status must be 0), a start of a HV ramp will be synchronized (a ramp is a software controlled, time proportionally increase / decrease of the output voltage).

A SetEmergencyOff switch the channel in state isEmergencyOff and a new SetOn is only possible after SetEmergencyOff is reset to zero

setEMCY	SetEmergencyOff	Set “Emergency Off”
setON	SetOn	Set On
res	Reserved	

setEMCY=0 channel emergency cut-off works
setEMCY=1 cut-off V_O shut off to 0V without ramp
setOn=0 switch the channel to OFF
setOn=1 switch the channel to ON

4.5.1.3 Channel event status (single write- and single/ multiple single read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	CHN	DATA_1	DATA_0
master write access	0	0x4002	M_x	ChannelEventStatus	
master read-	1	0x4002	M_x		
master single MBR read-	1	0x6002	Member		Offset
HV board write access	0	0x4002/0x6002	M_x	ChannelEventStatus	

Mx	Channel	0 ... 255
Member	Members	1 … 16
Offset	Channel member offset	0, 16, 32 … too access up to 255 channels
ChannelEventStatus	DATA_0 to DATA_1	UI2

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EVLIM	ECLIM	ETRP	EEINH	EVBNDs	ECBNDs	EAE	res	ECV	ECC	EEMCY	EEOR	EOn2Off	EIER	EARC	res

EVLIM	EventVoltageLimit	Event: Hardware- voltage limit has been exceeded
ECLIM	EventCurrentLimit	Event: Hardware- current limit has been exceeded
ETRP	EventTrip	Event: Trip is set when Voltage or Current limit or Iset has been exceeded (when KillEnable=1)
EEINH	EventExternalInhibit	Event external Inhibit
EVBNDs	EventVoltageBounds	Event: Voltage out of bounds
ECBNDs	EventCurrentBounds	Event: Current out of bounds
EAE	EventArcError	Event: Arc Error
ECV	EventControlledVoltage	Event: Voltage control
ECC	EventControlledCurrent	Event: Current control
EEMCY	EventEmergencyOff	Event: Emergency off
EEOR	EventEndOfRamp	Event: End of ramp
EOn2Off	EventOnToOff	Event: Change from state "On" to "Off" without ramp [1]
EIER	EventInputError	Event: Input Error
EARC	EventArc	Event: Arc active or Regulation Error (Option - fast error evaluation)

An event bit is permanently set if the status bit is 1 or is changing to 1. Different to the status bit an event bit isn't automatically reset. A reset has to be done by the user by writing an 1 to this event bit.

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4.5.1.4 Channel event mask (single write- and single/ multiple single read-write access)

EDCP frame: OPC ↑

Access	DATA_DIR	DATA_ID	CHN	DATA_1	DATA_0
master write access	0	0x4003	M_x	ChannelEventMask	
master read-	1	0x4003	M_x		
master single MBR read-	1	0x6003		Member	Offset
HV board write access	0	0x4003/0x6003	M_x	ChannelEventMask	

Mx	Channel	0 ... 255
Member	Members	1 … 16
Offset	Channel member offset	0, 16, 32 … too access up to 255 channels
ChannelEventMask	DATA_0 to DATA_1	UI2

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
MEVLIM	MECLIM	MECTRP	MEEINH	MEVBNDs	MECBNDs	MEARC	res	MECV	MECC	res	MEEOR	MEOn2Off	MEIERR	MEARC	res

The function of the ChannelEventMask register is described in 4.5.5.1Channel events

MEVLIM	MaskEventVoltageLimit	EventMask: Hardware- voltage limit has been exceeded
MECLIM	MaskEventCurrentLimit	EventMask: Hardware- current limit has been exceeded
METRIP	MaskEventTrip	EventMask: Voltage limit or Current limit or Iset has been exceeded (when KillEnable=1)
MEEINH	MaskEventExtInhibit	EventMask: External Inhibit
MEVBNDs	MaskEventVoltageBounds	EventMask: Voltage out of bounds
MECBNDs	MaskEventCurrentBounds	EventMask: Current out of bounds
MEARC	MaskEventArcError	EventMask: Arc error
MECV	MaskEventControlledVoltage	EventMask: Voltage control
MECC	MaskEventControlledCurrent	EventMask: Current control
MEEMCY	MaskEventEmergencyOff	EventMask: Emergency off
MEEOR	MaskEventEndOfRamp	EventMask: End of ramp
MEOn2Off	MaskEventOnToOff	EventMask: Change from state on to off without ramp
MEIER	MaskEventInputError	EventMask: Input Error
MARC	MaskEventArc MaskEventRegulationError	EventMask: Arc active EventMask: Regulation Error (Option - fast error evaluation)

All bits of the ChannelEventMask register are set to “0” after the power on reset.

Module in mode KILL disable:

If a bit of the ChannelEventStatus register is set to “1” and the corresponding bit in the ChannelEventMask register is “0” no reset of the ChannelEventStatus bits is necessary before switch on HV of the channel is possible again.

If a bit of the ChannelEventMask register is set to “1” and if the corresponding bit in the ChannelEventStatus is set to “1” by the module firmware then a reset of the corresponding ChannelEventStatus bits is necessary before a switch on the HV of this channel is possible again.

Module in mode KILL enable: A reset of the ChannelEventStatus bits is necessary before switch on the HV of this channel again.

4.5.1.5 Delayed trip action (single/ multiple single read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	CHN	DATA_0	DATA_1 | DATA_2	
master write access	0	0x4005	Mx	Action		
master read -	1	0x4005	M_x			
master single MBR write-	1	0x6005	Member		Offset	Action
HV board write access	0	0x4005	M_x	Action		

Mx	Channel 0 ... 255	
Member	Members 1 … 16	
Offset	Channel member offset	0, 16, 32 … access up to 255 channels
Action	Action if a trip event will be initiated	0 – no action 1 – ramp down high voltage of the channel 2 – switch off high voltage of the channel without a ramp 3 – switch off the whole module without any ramp 4 – switch off the delayed trip function

4.5.1.6 Delayed trip time

EDCP frame:

Access	DATA_DIR	DATA_ID	CHN	DATA_1	DATA_0
master single read-	1	0x4006	M_x		
master single MBR read-	1	0x6006	Member		Offset
HV board write access	0	0x4006/0x6006	M_x	Timeout-time	

Mx	Channel	0 ... 255
Member	Members	1 … 16
Offset	Channel member offset	0, 16, 32 … too access up to 255 channels
Timeout-time	DATA_0 to DATA_1[ms]	UI2 (Range 1 to 4095 ms)

Time is ms until delayed trip action becomes active and channel is in current control state. Note special functionality for modules with a second low current range – see manual “Delayed trip EHS.pdf”.

4.5.1.7 External channel inhibit

EDCP frame:

Access	DATA_DIR	DATA_ID	CHN	DATA_0	DATA_1 | DATA_2	
master write access	0	0x4007	Mx	Action		
master read -	1	0x4007	M_x			
master single MBR write-	1	0x6007	Member		Offset	Action
HV board write access	0	0x4007/0x6007	M_x	Action		

Mx	Channel	0 ... 255
Member	Members	1 … 16
Offset	Channel member offset	0, 16, 32 … access up to 255 channels
Action	Action if an inhibit signal will be triggered	0 – no action 1 – ramp down high voltage of the channel 2 – switch off high voltage of the channel without a ramp 3 – switch off the whole module without any ramp 4 – switch off the delayed trip function

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4.5.1.8 Set voltage (single write- and single/ multiple single read-write access)

EDCP frame: OPC SNMP ↑

Access	DATA_DIR	DATA_ID	CHN	DATA_3	DATA_2	DATA_1	DATA_0
master write access	0	0x4100	M_x	VoltageSet			
master read -	1	0x4100	M_x				
master single MBR read-	1	0x6100	Member		Offset		
HV board write access	0	0x4100/0x6100	M_x	VoltageSet			

Mx	Channel	0 ... 255
Member	Members	1 … 16
Offset	Channel member offset	0, 16, 32 … too access up to 255 channels
VoltageSet	DATA_0 to DATA_3 [V]	R4

The VoltageSet values is the preset for voltage regulation. Allowed values are between 0 and the actual hardware limit value. If written values are between the hardware limit and the nominal value, then the module reduces these values to the value of the actual hardware limit. If written values are higher than the nominal data or lower than 0 an input error is indicated by setting the bit InputError.

If the channel is switched ‘ON’ then the voltage will be ramped to the set value after the receipt of this access. Otherwise the set value will just be stored and only used for ramping to the set voltage after the channel will be switched ‘ON’.

4.5.1.9 Set current / trip (single write- and single/ multiple single read-write access)

EDCP frame: OPC SNMP ↑

Access	DATA_DIR	DATA_ID	CHN	DATA_3	DATA_2	DATA_1	DATA_0
master write access	0	0x4101	M_x	CurrentSet (CurrentTrip)			
master read -	1	0x4101	M_x				
master single MBR read-	1	0x6101	Member		Offset		
HV board write access	0	0x4101/0x6101	M_x	CurrentSet (CurrentTrip)			

Mx	Channel	0 ... 255
Member	Members	1 … 16
Offset	Channel member offset	0, 16, 32 … too access up to 255 channels
CurrentSet (CurrentTrip)	DATA_0 to DATA_3 [A]	R4

Allowed values are between 0 and the actual hardware limit value. If written values are between the hardware limit and the nominal value, then the module reduces these values to the value of the actual hardware limit. If written values are higher than the nominal data or lower than 0 an input error is indicated by setting the bit InputError.

The mode of action of this item depends on the setting of the signal Kill Enable (KILEna) in the ModuleControl register (4.5.2.2). If Kill Enable is 0, the value is interpreted as CurrentSet. if Kill Enable is 1, the value is CurrentTrip.

CurrentSet:

The CurrentSet value is the preset for current regulation. If the output current reaches or exceeds the Current Set value, the channel goes into Current Regulation mode. In this mode the output current is regulated at the CurrentSet value, but the output voltage is going to a value between 0V and Vset, depending of the external load.

When Current Control mode is active the bit isCC of the ChannelStatus register and the bit EventControlledCurrent of the ChannelEventStatus are set, the bit isCV of the ChannelStatus is reset.

CurrentTrip:

In Current Trip mode this value will be used as software current trip. If exceeding this value a current trip event will be registered. The green LED on front panel will be switched off.

The bits isTrip in the ChannelStatus and ETRP in ChannelEventStatus are set, the bit isNoSumError in the ModuleStatus is reset.

4.5.1.10 Voltage measurement (single/ multiple single read-write access)

EDCP frame: OPC SNMP ↑

Access	DATA_DIR	DATA_ID	CHN	DATA_3	DATA_2	DATA_1	DATA_0
master read -	1	0x4102	M_x				
master single MBR read-	1	0x6102	Member		Offset		
HV board write access	0	0x4102/0x6102	M_x	VoltageMeasure			

Mx	Channel	0 ... 255
Member	Members	1 … 16
Offset	Channel member offset	0, 16, 32 … access up to 255 channels
VoltageMeasure	DATA_0 to DATA_3 [V]	R4

4.5.1.11 Current measurement (single/ multiple single read-write access)

EDCP frame: OPC SNMP ↑

Access	DATA_DIR	DATA_ID	CHN	DATA_3	DATA_2	DATA_1	DATA_0
master read -	1	0x4103	M_x				
master single MBR read-	1	0x6103	Member		Offset		
HV board write access	0	0x4103/0x6103	M_x	CurrentMeasure			

Mx	Channel	0 ... 255
MBR	Members	1 … 16
OFFSET	Channel member offset	0, 16, 32 … access up to 255 channels
CurrentMeasure	DATA_0 to DATA_3 [A]	R4

4.5.1.12 Voltage bounds (single write- / single/ multiple single read-write access)

EDCP frame: ↑

Access	DATA_DIR	DATA_ID	CHN	DATA_3	DATA_2	DATA_1	DATA_0
master write access	0	0x4104	M_x	VoltageBounds			
master read -	1	0x4104	M_x				
master single MBR read-	1	0x6104	Member		Offset		
HV board write access	0	0x4104/0x6104	M_x	VoltageBounds			

Member	Members	1 … 16
Offset	Channel member offset	0, 16, 32 … access up to 255 channels
VoltageBounds	DATA_0 to DATA_3 [V] (0 to VoltageNominal)	R4

4.5.1.13 Current bounds (single write- / single/ multiple single read-write access)

EDCP frame: ↑

Access	DATA_DIR	DATA_ID	CHN	DATA_3	DATA_2	DATA_1	DATA_0
master write access	0	0x4105	M_x	CurrentBounds			
master read -	1	0x4105	M_x				
master single MBR read-	1	0x6105	Member		Offset		
HV board write access	0	0x4105/0x6105	M_x	CurrentBounds			

Mx	Channel	0 ... 255
Member	Members	1 … 16
Offset	Channel member offset	0, 16, 32 … access up to 255 channels
CurrentBounds	DATA_0 to DATA_3 [A] (0 to CurrentNominal)	R4

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4.5.1.14 Nominal voltage (single/ multiple single read-write access)

EDCP frame: OPC SNMP ↑

Access	DATA_DIR	DATA_ID	CHN	DATA_3	DATA_2	DATA_1	DATA_0
master read -	1	0x4106	M_x				
master single MBR read-	1	0x6106	Member		Offset		
HV board write access	0	0x4106/0x6106	M_x	VoltageNominal			

Mx	Channel	0 ... 255
Member	Members	1 … 16
Offset	Channel member offset	0, 16, 32 … access up to 255 channels
VoltageNominal	DATA_0 to DATA_3 [V]	R4

4.5.1.15 Nominal current (single/ multiple single read-write access)

EDCP frame: OPC SNMP ↑

Access	DATA_DIR	DATA_ID	CHN	DATA_3	DATA_2	DATA_1	DATA_0
master read -	1	0x4107	M_x				
master single MBR read-	1	0x6107	Member		Offset		
HV board write access	0	0x4107/0x6107	M_x	CurrentNominal			

Mx	Channel	0 ... 255
Member	Members	1 … 16
Offset	Channel member offset	0, 16, 32 … access up to 255 channels
CurrentNominal	DATA_0 to DATA_3 [A]	R4

4.5.1.16 Current measurement range* (single/ multiple single read-write access)

EDCP frame: ↑

Access	DATA_DIR	DATA_ID	CHN	DATA_4	DATA_3	DATA_2	DATA_1	DATA_0
master read -	1	0x4109	M_x					
master single MBR read-	1	0x6109	Member		Offset			
HV board write access	0	0x4109/0x6103	M_x	CurrentMeasure				Range

Mx	Channel	0 ... 255
Member	Members	1 … 16
Offset	Channel member offset	0, 16, 32 … access up to 255 channels
CurrentMeasure	DATA_1 to DATA_4 [A]	R4
Range	DATA_0=0 – high range (≥20µA)	UI1
	DATA_0=1 – low range (<20µA)	

(* for device class 26, 27 and 39, E08F2, E08C2 and N06C2 only)

4.5.1.17 VCT Coefficient* (single/ multiple single read-write access)

EDCP frame: ↑

Access	DATA_DIR	DATA_ID	CHN	DATA_3	DATA_2	DATA_1	DATA_0
master read -	1	0x4120	M_x				
master single MBR read-	1	0x6120	Member		Offset		
HV board write access	0	0x4120/0x6120	M_x	VctCoefficient			

Mx	Channel	0 ... 255
Member	Members	1 … 16
Offset	Channel member offset	0, 16, 32 … access up to 255 channels
VctCoefficient	**DATA_0 to DATA_3 [V/K]**	**R4**

(* Option VCT only)

4.5.1.18 Temperature external* (single/ multiple single read-write access)

EDCP frame: ↑

Access	DATA_DIR	DATA_ID	CHN	DATA_3	DATA_2	DATA_1	DATA_0
master read -	1	0x4121	M_x				
master single MBR read-	1	0x6121	Member		Offset		
HV board write access	0	0x4121/0x6121	M_x	TemperatureExternal			

Mx	Channel	0 ... 255
Member	Members	1 … 16
Offset	Channel member offset	0, 16, 32 … access up to 255 channels
TemperatureExternal	DATA_0 to DATA_3 [°C]	R4

(* Option VCT only)

4.5.1.19 Group number (single/ multiple single read-write access)

EDCP frame: ↥

Access	DATA_DIR	DATA_ID	CHN	DATA_0		
master write access	0	0x4200	Mx	GROUP		
master read -	1	0x4200	M_x			
master single MBR write-	1	0x6200	Member		Offset	Group
HV board write access	0	0x4200	M_x	GROUP		

Mx	Channel	0 ... 255
Member	Members	1 … 16
Offset	Channel member offset	0, 16, 32 … access up to 255 channels
Group	Group number of the channel members	0 .. 255

With a group number **GROUP** for each channel can combine channels to a group involving all connected modules. The **NMT channel group set** and the **NMT module set** frames (described on page 19) send broadcast information for all channels, which have the same group number.

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4.5.1.20

4.5.2 EDCP Module Accesses

4.5.2.1 ModuleStatus (module read-write access)

EDCP frame: OPC ↑

Access	DATA_DIR	DATA_ID	DATA_1	DATA_0
master read-	1	0x1000		
HV board write access	0	0x1000	ModuleStatus	

ModuleStatus DATA_0 to DATA_1 UI2

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
isKillE	isTmpGd	isSplyGd	isModGd	isEvntAct	isSflpGd	isNoRamp	isNoSumErr	res	isInErr	isHwVlGd	needSrvc	isHvOn	isLvIns	res	isAdj

The status bits as there are IsTemperatureGood, IsSupplyGood, IsModuleGood, IsEventActive, IsSafetyLoopGood, IsNoRamp and IsNoSumError indicate the single status for the complete module.

The status bit IsCommandComplete indicates whether all CAN commands given to the module have been executed.

isKillE	IsKillEnable	Module state of kill enable
isTmpGd	IsTemperatureGood	Module temperature good
isSplyGd	IsSupplyGood	Power supply good
isModGd	IsModuleGood	Module in state good
isEvntAct	IsEventActive	Any event is active and mask is set
isSflpGd	IsSafetyLoopGood	Safety loop closed
isNoRamp	IsNoRamp	All channels stable, no ramp active
isNoSumErr	IsNoSumError	All channels without failure
isInErr	IsInputError	Input error in connection with a module access
isHwVlGd	IsHardwareVoltageLimitGood	Hardware voltage limit in proper range, forHV distributor modules with current mirror only
needSrvc	IsServiceNeeded	Hardware failure detected (consult iseg Spezialelektronik GmbH)
isHvOn	IsHighVoltageOn	At least one channel generates a high voltage
isLvIns	IsLiveInsertion	Mode live insertion
isAdj	IsFineAdjustment	Mode of the fine adjustment
res	Reserved	

isKillEna=0 Module in state kill disable
isKillEna=1 Module in state kill enable
isTmpGd=0 If module temperature is higher than 55°C then all channel are switched off permanently
isTmpGd=1 module temperature is within working range
isSplyGd=0 supply voltages are out of range (range of24V +/-10% and of 5V +/-5%)
isSplyGd=1 supply voltages are within range
isModGd=0 module is not good, that means (isnoSERR AND (ETMPngd OR ESPLYngd OR ESFLPngd))==0
isModGd=1 module is good, that means (isnoSERR AND NOT(ETMPngd OR ESPLYngd OR ESFLPngd))==1(see module event status also)
isEvntAct=0 no Event is active
isEvntAct=1 any Event is active
isSflpGd=0 safety loop is broken -V_O bas been shut off,
isSflpGd=1 safety loop is closed
isNoRamp=0 V_O is ramping in at least one channel
isNoRamp=1 no channel is ramping

isNoSumErr=0 voltage limit, current limit, trip, voltage bound or current bound has been exceeded in at least one of the channels or external INHIBIT ⇒ error, reset by reset of the corresponding flag of the channel status'
isnoSumERR=1 evaluation of the 'Channel Status' over all channels to a sum error flag ⇒ LIM&CLIM&CTRP&EINH&VBND&CBND=0 ⇒ no errors
isInErr=1 input error in connection with a module access
isInErr=0 no input error in connection with a module access
isHwVlGd=0 hardware voltage limit not in proper range
isHwVlGd=1 hardware voltage limit in proper range
needSrvc=0 Module is ready for working.
needSrvc=1 Module need a service.
isHvOn=0 No high voltage will be generated
isHvOn=1 At least one channel generates a high voltage output.
Modules with 7 digit serial number only.
isLvIns=0 no Live Insertion mode
isLvIns=1 Live Insertion mode
isAdj=0 Fine adjustment is off.
isAdj=0 Fine adjustment is on (default).

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4.5.2.2 ModuleControl (module write- / read-write access)

EDCP frame: OPC SNMP ↑

Access	DATA_DIR	DATA_ID	DATA_1	DATA_0
master write	0	0x1001	ModuleControl	
master read-	1	0x1001		
HV board write access	0	0x1001	ModuleControl	

ModuleControl DATA_0 to DATA_1 UI2

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
res	setKILena	res	setADJ	set ENDN	res	res	res	res	doCLEAR	setILK	res	res	res	res	res

setKILena	KillEnable	Kill function
setADJ	Adjust	Switch ON of fine adjustment
setENDN	Endian	Order of bytes in word: 0 = Little Endian (INTEL); 1 = Big Endian (MOTOROLA)
doCLEAR	ClearKill	Hardware ClearKill signal and clear all event signals of the module and the channels
setILK	Interlock	Interlock signal CRATE_ENABLE (WIENER MPOD crate, active TTL high)
res	Reserved	

setKILL=0 kill function disable
setKILL=1 kill function enable
setADJ=0 fine adjustment OFF
setADJ=1 fine adjustment ON
setENDN=1 big endian (MOTOROLA format)
doCLEAR=1 Hardware ClearKill signal and clear all event signals of the module and the channels
doCLEAR=0 no action
setILK= 1 INTERLOCK signal in order to switch off HV and set bit EEINH of the EventStatus for all channels
setILK=0 reset the INTERLOCK signal in order to clear the bit EEINH of the EventStatus for all channels

4.5.2.3 ModuleEventStatus (module write- / read-write access)

EDCP frame: OPC SNMP ↑

Access	DATA_DIR	DATA_ID	DATA_1	DATA_0
master write	0	0x1002	ModuleEventStatus	
master read-	1	0x1002		
HV board write access	0	0x1002	ModuleEventStatus	

ModuleEventStatus DATA_0 to DATA_1 UI2

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
res	ETMPngd	ESPLYngd	res	res	ESFLPngd	res	res	res	EIERR	EHwVLngd	ESrvc	res	ELVINS	res	res

ETMPngd	EventTemperatureNotGood	Event: Temperature is above 55°C
ESPLYngd	EventSupplyNotGood	Event: at least one of the supplies is not good
ESFLPngd	EventSafetyLoopNotGood	Event: Safety loop is open
EIERR	EventInputError	Event: input error in connection with a module access
EHwVLngd	EventHardwareVoltageLimitNotGood	Event: Hardware voltage limit is not in proper range, only for HV distributor modules with current mirror;
ESrvs	EventService	Event: A hardware failure of the HV module has been detected. The HV will switched off without a possibility to switch on again. Please consult the iseg Spzialelektronik GmbH.
ELVINS	EventLiveInsertion	Event live insertion to prepare a hot plug of a module
res	Reserved	

4.5.2.4 ModuleEventMask (module write- / read-write access)

EDCP frame: OPC ↑

Access	DATA_DIR	DATA_ID	DATA_1	DATA_0
master write	0	0x1003	ModuleEventMask	
master read-	1	0x1003		
HV board write access	0	0x1003	ModuleEventMask	

ModuleEventMask DATA_0 to DATA_1 UI2

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
res	METMPngd	MESPLYngd	res	res	MESFLPngd	res	res	res	MEIERR	MEHwVLngd	res	res	res	res	res

METMPngd	MaskEventTemperatureNotGood	MEventMask: Temperature is above 55°C
MESPLYngd	MaskEventSupplyNotGood	MEventMask: at least one of the supplies is not good
MESFLPngd	MaskEventSafetyLoopNotGood	MEventMask: Safety loop (SL) is open
MEIERR	MaskEventInputError	MEventMask: Input error in connection with a module access
MEHwVLngd	MaskEventHardwareVoltageLimitNotGood	MEventMask: Hardware voltage limit is not in proper range, only for HV distributor modules with current mirror;
res	Reserved	

All bits of the EventMask register are set to “0” after the power on reset.

Module in mode KILL enable: If a bit of the EventStatus register is set to “1” and the corresponding bit in the EventMask register is “0” no reset of the EventStatus bits is necessary before switch on the HV of any channel again.

If a bit of the EventMask register is set to “1” and if the corresponding bit in the EventStatus is set to “1” by the module firmware a reset of the corresponding EventStatus bits is necessary before a switch on the HV of any channel is possible.

Module in mode KILL enable: A reset of the EventStatus bits is necessary before switch on the HV of any channel is possible.

4.5.2.5 ModuleEventChannelStatus (module write- / read-write access)

EDCP frame: OPC ↑

Access	DATA_DIR	DATA_ID	DATA_2	DATA_1	DATA_0
master write access	0	0x1004	OFFSET	ModuleEventChannelStatus	
master read-	1	0x1004	OFFSET		
HV board write access	0	0x1004	OFFSET	ModuleEventChannelStatus	

OFFSET DATA_2Channel member offset 0, 16, 32 … access up to 255 channels

EventChannelStatus DATA_0 to DATA_1 UI2

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CH15	CH14	Ch13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

The n-th bit of the register is set, if an event is active in the n-th channel and the associated bit in the EventMask register of the n-th channel is set too.

CHn = EventStatus[n] & EventMask[n]

Reset of a bit is done by writing a 1 to this bit.

4.5.2.6 ModuleEventChannelMask (module write- / read-write access)

EDCP frame: OPC ↑

Access	DATA_DIR	DATA_ID	DATA_2	DATA_1	DATA_0
master write access	0	0x1005	OFFSET	ModuleEventChannelMask	
master read-	1	0x1005	OFFSET		
HV board write access	0	0x1005	OFFSET	ModuleEventChannelMask	

OFFSET DATA_2Channel member offset 0, 16, 32 … access up to 255 channels

EventChannelMask DATA_0 to DATA_1 UI2

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CH15	CH14	Ch13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

This register decides whether a pending event leads to the sum event flag of the module or not. If the n-th bit of the mask is set and the n-th channel has an active event in the ModuleEventChannelStatus the bit isEventActive in the ModuleStatus register is set

4.5.2.7 ModuleEventGroupStatus (module write- / read-write access)

↥

EDCP frame:

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master write access	0	0x1005	ModuleEventGroupStatus			
master read-	1	0x1005				
HV board write access	0	0x1005	ModuleEventGroupStatus			

EventGroupStatus	DATA_0 to DATA_3	UI4

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
GR31	GR30	GR29	GR28	GR27	GR26	GR25	GR24	GR23	GR22	GR21	GR20	GR19	GR18	GR17	GR16

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
GR15	GR14	GR13	GR12	GR11	GR10	GR9	GR8	GR7	GR6	GR5	GR4	GR3	GR2	GR1	GR0

The n-th bit of this double word register is set, if an event is active in the n-th group.

Reset of a bit is done by writing a 1 to this bit.

4.5.2.8 ModuleEventGroupMask (module write- / read-write access)

EDCP frame: ↑

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master write access	0	0x1006	ModuleEventGroupMask			
master read-	1	0x1006				
HV board write access	0	0x1006	ModuleEventGroupMask			

EventGroupMask DATA_0 to DATA_3 UI4

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
GR31	GR30	GR29	GR28	GR27	GR26	GR25	GR24	GR23	GR22	GR21	GR20	GR19	GR18	GR17	GR16

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
GR15	GR14	GR13	GR12	GR11	GR10	GR9	GR8	GR7	GR6	GR5	GR4	GR3	GR2	GR1	GR0

This register decides whether a pending event leads to the sum event flag of the module or not. If the n-th bit of the mask is set and the n-th group has an active event in the ModuleEventGroupStatus the bit isEventActive in the ModuleStatus register is set.

4.5.2.9 VoltageRampSpeed (module write- / read-write access)

EDCP frame: OPC SNMP ↑

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master write access	0	0x1100	VoltageRampSpeed			
master read -	1	0x1100				
HV board write access	0	0x1100	VoltageRampSpeed			

VoltageRampSpeed DATA_0 to DATA_3 [%] R4

Voltage ramp speed range (disable Kill): 1mV/s ≤ Ramp speed ≤ 20% of $V_{O\,max}$/s

Option: fast ramp 1 1mV/s ≤ Ramp speed ≤ 25% of VoltageNominal

2 1mV/s ≤ Ramp speed ≤ 50% of VoltageNominal

3 1mV/s ≤ Ramp speed ≤ 75% of VoltageNominal

Voltage ramp speed range (enable Kill): 1mV/s ≤ Ramp speed ≤ 1% of $V_{O\,max}$/s

The speed of the voltage ramp in percent of the nominal voltage of the channel per second.

4.5.2.10 CurrentRampSpeed – current controlled modules only (module write- / read-write access)

EDCP frame: OPC SNMP ↑

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master write access	0	0x1101	CurrentRampSpeed			
master read -	1	0x1101				
HV board write access	0	0x1101	CurrentRampSpeed			

CurrentRampSpeed DATA_0 to DATA_3 [%] R4

Current ramp speed range: 2 % $I_{O\,max}$/s ≤ Ramp speed ≤ $I_{O\,max}$/s

The speed of the current ramp in percent of the nominal current of the channel per second.

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4.5.2.11 VoltageMax – OPTION (module read-write access)

EDCP frame: OPC ↑

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master read -	1	0x1102				
HV board write access	0	0x1102	VoltageMax			

HardwareVoltageLimit DATA_0 to DATA_3 [%] R4

HV Modules with the OPTION hardware voltage limit can adjust $V_{O\,max}$ via the potentiometer V_{max}.

For HV Modules without this OPTION VoltageMax equals to $V_{O\,max}$.

The exceeding of the hardware voltage limit results in a limitation of the voltage when the KILL-enable.

The absolute value of the hardware voltage limit will compute by following:

Voltage limit of the channel x (Chx) = VoltageNominal[Chx] * VoltageMax

The module responds after the hardware voltage limit has been exceeded:

The green LED on front panel is off.

Depends of the kind of module:

Hardware KILL function controlled by the bit 'KILena' of the ModuleControl word:

KILL-enable = 1: The voltage will be switched off permanently without ramp. ChannelEventStatus flag 'EVLIM' will be set.
KILL-enable = 0: The voltage will be reduced to the value of the actual hardware voltage limit. ChannelStatus flag 'isVLIM' and ChannelEventStatus flag 'EVLIM' will be set.

Software KILL function controlled by the bit 'KILena' of the ChannelControl word:

KILL-enable = 1: Voltage will be switched off permanently without ramp. ChannelEventStatus flag 'EVLIM' will be set.
KILL-enable = 0: Voltage will be switched off without ramp. If the output voltage arrives at 0 V the ramping to set voltage will be restarted automatically. ChannelStatus flag 'isVLIM' and ChannelEventStatus flag 'EVLIM' will be set.

4.5.2.12 CurrentMax – OPTION (module read-write access)

EDCP frame: OPC ↑

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master read -	1	0x1103				
HV board write access	0	0x1103	CurrentMax			

HardwareCurrentLimit DATA_0 to DATA_3 [%] R4

HV Modules with the OPTION CurrentMax can adjust the $I_{O\,max}$ via the potentiometer I_{max}.

HV Modules without this OPTION deliver $I_{O\,max}$.

The absolute value of the hardware current limit will compute by following:

Current limit of the channel x (Chx) = CurrentNominal[Chx] * CurrentMax

The module responds after the hardware current limit has been exceeded:

The green LED on front panel is off.

Depends of the kind of module:

Hardware KILL function controlled by the bit 'KILena' of the ModuleControl word:

KILL-enable = 1: Voltage will be switched off permanently without ramp. ChannelEventStatus flag 'ECLIM' will be set.
KILL-enable = 0: Current will be reduced to the value of the actual hardware current limit. ChannelStatus flag 'isCLIM' and ChannelEventStatus flag ECLIM will be set.

Software KILL function controlled by the bit 'KILena' of the ChannelControl word:

KILL-enable = 1: Voltage will be switched off permanently without ramp. ChannelEventStatus flag ECLIM will be set.
KILL-enable = 0: Voltage will be switched off without ramp. If the output voltage arrives at 0 V the ramping to set voltage will be restarted automatically. ChannelStatus flag 'isCLIM' and ChannelEventStatus flag ECLIM will be set.

4.5.2.13 Supply24 (module read-write access)

EDCP frame: OPC ↑

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master read -	1	0x1104				
HV board write access	0	0x1104	Supply24			

Supply24 DATA_0 to DATA_3 [V] R4

An ‘out of range error’ (see DCP group access: General status) will be generated if deviation of voltage is more than ±10%.

4.5.2.14 Supply5 (module read-write access)

EDCP frame: OPC ↑

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master read -	1	0x1105				
HV board write access	0	0x1105	Supply5			

Supply5 DATA_0 to DATA_3 [V] R4

An ‘out of range error’ (see DCP group access: General status) will be generated if deviation of voltage is more than ±5%.

4.5.2.15 BoardTemperature (module read-write access)

EDCP frame: OPC SNMP ↑

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master read -	1	0x1106				
HV board write access	0	0x1106	BoardTemperature			

BoardTemperature DATA_0 to DATA_3 [°C] R4

An ‘out of range error’ (see group access: General status) will be generated if the temperature is higher than +55°C.

4.5.2.16 Threshold to arm the errors detection (module write / read- write access)

EDCP frame: OPC ↑

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master write access	0	0x1107	ThresholdArmErrorDetection			
master read -	1	0x1107				
HV board write access	0	0x1107	ThresholdArmErrorDetection			

ThresholdArmErrorDetection DATA_0 to DATA_3 [%] R4

Factory setting for different kinds of HV modules is between 1V and to $V_{O\,max}$/10 in percent to the nominal voltage of the channel.

The arming of the error detection is started while the actual voltage exceeds these value which has been stored before.

Exception: At the start of a ramp from zero the firmware evaluates that the feedback control will look in. If not, because the channel has a short or the hardware current limit is near to zero, then the channel will be switched off and a current error will be generated before the actual voltage is exceeding these threshold.

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4.5.2.17 Serial number (module read-write access)

EDCP frame: OPC ↑

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master read -	1	0x1200				
HV board write access	0	0x1200	SerialNumber			

SerialNumber DATA_0 to DATA_3 UI4

serial number e.g. 471212

4.5.2.18 Firmware release (module read-write access)

EDCP frame: OPC ↑

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master read -	1	0x1201				
HV board write access	0	0x1201	FrimwareRelease			

FirmwareRelease DATA_0 to DATA_3 UI1[4]

release e.g. 01.00.00.00

4.5.2.19 Bit rate (module write- / read-write access)

EDCP frame: OPC ↑

Access	DATA_DIR	DATA_ID	DATA_1	DATA_0
master read-	1	0x1202		
HV board write access	0	0x1202	BitRate	

BitRate DATA_0 to DATA_1 [kbit/s] UI2

Following bit rates are possible: 20, 50, 100, 125, 250 kbit/s (500 and 1000 kbit/s on request)

The new bit rate gets active after RESET or POWER OFF/ON. The bit rate of all modules in the system must be the same before a RESET or POWER/ON is made.

- The bit rate is set to 250 kbit/s ex works.
- Invalid bit rates will be ignored and the bit 'Input error' of the 'Status channel 0' will be set.
- A correct write access storing the information permanently if a NMT stop has been sent before.

4.5.2.20 Name of firmware (module read-write access)

EDCP frame: ↑

Access	DATA_DIR	DATA_ID	DATA_4/5	DATA_3	DATA_2	DATA_1	DATA_0
master write	0	0x1203	NameOfFirmware				
master read-	1	0x1203					
HV board write access	0	0x1203	NameOfFirmware				

NameOfFirmware DATA_0 to DATA_3 [ASCII] BSTR

BSTR	Description
"E16D0"	EDS 16 channel per PCB, distributor module, range of Vmax from $V_{O\,max}$ to ($V_{O\,max}$ - 1kV)
"E16D1"	EDS 16 channel per PCB, distributor module
"E08C0"	EHS 8 channel per PCB, common GND module
"E08F0"	EHS 8 channel per PCB, floating GND module
"E08F2"	EHS 8 channel per PCB, floating GND module, 2 ranges for measurement of current
"E08C2"	EHS 8 channel per PCB, common floating GND module, 2 ranges for measurement of current
"E16C1	EHS 16 channel per PCB or 32 channels per module, common GND module
"E24D1"	EDS 24 channel per PCB, distributor module
"N06C2"	NHS NIM 6 channel module, common GND module, 2 ranges for measurement of current
"MICC"	MICC Multi channel Interface Crate Controller is a remote control interface for MMC Crates
"MICP"	MICP Multi channel Interface Crate PHQ Controller is a remote control interface for MMC Crates
"H101C0"	HPS 19", 1 channel HV Power Supply (300W, 800W)
"H101C1"	HPS 19" 1 channel HV Power Supply 1.5kW - 10kW
"H201C0"	HPS compact 1channel HV Power Supply (350W)

4.5.2.21 ADC SamplesPerSecond SPS (module write- / read-write access)

EDCP frame: ↑

Access	DATA_DIR	DATA_ID	DATA_1	DATA_0
master write	0	0x1204	SamplesPerSecond	
master read-	1	0x1204		
HV board write access	0	0x1204	SamplesPerSecond	

SamplesPerSecond DATA_0 to DATA_1 [SPS] UI2 (possible SPS are 500, 100, 60, 50, 25, 10 and 5)

Adjusts the number of averages of the programmable ADC filter of the HV modules. Possible values are 500, 100, 60 and 50 SPS. Notch should be set with 60 SPS using a 110V line with 60Hz and 50 SPS using a 230V line with 50Hz in order to improve the common-mode rejection of these frequencies. However a SPS value of the ADC will increase the main loop time by 4*1/SPS for devices “E08F0”, “E08F2” (see 4.5.2.20) respectively by 4*1/SPS multiplied with the number of channels for device “E16D0”, “E08C0” (see 4.5.2.20).

Factory settings: E16D0, E08C0, E16C1, E08F0: 500 SPS
E08F2, E08C2: 50 SPS.

4.5.2.22 DigitalFilter (module write- / read-write access)

EDCP frame: ↑

Access	DATA_DIR	DATA_ID	DATA_1	DATA_0
master write	0	0x1205	NumberOfSteps	
master read-	1	0x1205		
HV board write access	0	0x1205	NumberOfSteps	

NumberOfSteps DATA_0 to DATA_1 [Steps] UI2 (possible steps are 1, 16, 64, 256,512 and 1024)

The digital filter in the firmware of the processor reduces the white noise of the analog values of channel VoltageMeasure, channel CurrentMeasure. The digital filtering gives the possibility to get a higher precision and to react fast on changes of the measured values. The filter is not used during a voltage ramp. The filter is restarted after a significant change of the signal.

Factory settings: 64

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4.5.2.23 ModuleOption (module read access)

EDCP frame: OPC ↑

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master read -	1	0x1280				
HV board write access	0	0x1280	ModuleOption			

ModuleOption DATA_0 to DATA_3 UI4

The requested value of the module option is not vailid when all bits are set to '1'!

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
EDCP	-	-	-	-	HVBPM	CLIM	VLIM	INHIBIT	RELAY	FRAMP	-	-	-	-	-

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

BIT	OPTION	DESCRIPTION	SPECIFICATION
Bit31	EDCP	Enhanced Device Control Protocol	no
Bit26	HVBM	HV boards per (CAN nodes) module	no
Bit25	CLIM	hardware current limit	no
Bit24	VLIM	hardware voltage limit	no
Bit23	INHIB	external INHIBIT signals	no
Bit22	RELY	discharge relay	no
Bit21	FRMP	fast ramp	yes

4.5.2.24 ModuleOptionSpec (module read access)

EDCP frame: OPC ↑

Access	DATA_DIR	DATA_ID	DATA_4	DATA_3	DATA_2	DATA_1	DATA_0
master read -	1	0x1290	DATA_4	DATA_3	DATA_2	DATA_1	
HV board write access	0	0x1290	ModuleOption				Spec

ModuleOption DATA_1 to DATA_4 UI4
Specification DATA_0 UI1

The requested value of the module option specification is not valid or do not exist when all bits are set to '1' or '0'!

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
EDCP	-	-	-	-	HVBPM	CLIM	VLIM	INHIBIT	RELAY	FRAMP	-	-	-	-	-

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

T**o request a specification the corresponding bit of the module option word has to be set to '1'.**

Specification:	fast ramp	1	25% of VoltageNominal
		2	50% of VoltageNominal
		3	75% of VoltageNominal

4.5.2.25 ModuleCommMode (module write access)

EDCP frame: OPC ↑

Access	DATA_DIR	DATA_ID	DATA_1	DATA_0
HV board write access	0	0x12a0	ModuleCommMode	

ModuleOption DATA_0 to DATA_3 UI2

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	FAST

Bit0	FAST	1	Fast communication mode (supported from isegHVOPCServer, isegCANHVControl)
		0	common mode

4.5.3 EDCP Group Accesses

The Multi Channel CAN module offers an extended and flexible range of group functions. There exist both predefined (so called fix) groups and variable groups.
Each group definition consists of 2 words each of 16 bits. In fix groups these 2 words are the value to be set into all channels (in float format) or they are a logical information. In variable groups one word carries the information about type and characteristics of the goup, the other word carries the information about the members of the group or gives an overview about a selected situation in all channels.

Four different grouptypes for variable groups have been established:

- Set group
- Status group
- Monitoring group
- Trip group

4.5.3.1 Set group

Set groups will be used in order to set channels to a same value, which happen to carry the identical channel value. Therefore within the group following will be defined:

- Member of the group: Each member will be activated in the channel setting list **ChSetLst**
- Type of the group: Set group type **TypeSet**
- Channel characteristics: Coding of characteristics, which have to be set commonly
- Control mode: Divides between a one-time setting of the slave channel property and a permanently copying of the Master channel's property to the slave channels
- Master channel: Number of the channel, which characteristics will be transferred to the other channels. Is just necessary for Set groups which set a value. If functions have to be initialized e.g. start of ramp then there is no Master channel

EDCP frame: OPC ↑

Access	DATA_DIR	DATA_ID	NBR	OFFSET	DATA_3	DATA_2	DATA_1	DATA_0
master group write	0	0x2000	N_x	O_x	**ChSetLst**		**TypeSet**	
master group read-	1	0x2000	N_x	O_x				
HV board write access	0	0x2000	N_x	O_x	**ChSetLst**		**TypeSet**	

Nx — Group number — 0 ... 31
O_x — Channel member offset — 0, 16, 32 … too access up to 255 channels
ChSetLst — DATA_2 to DATA_3 ChannelSettingList — members 0x1 … 0xffff — UI2

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

TypeSet — DATA_0 to DATA_1 TypeSet — UI2

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TYPE1	TYPE0	res	res	res	res	res	MOD0	SET3	SET2	SET1	SET0	MCH3	MCH2	MCH1	MCH0

TYPE1	TYPE0	Value	
0	0	SetGroupType	Group is defined as Set group

MOD0	Value	
0	0	The group function is done one time
1	1	The group function is done permanently

SET3	SET2	SET1	SET0	Value	
0	0	0	1	SetVset	Copy Vset from MCH to all members
0	0	1	0	SetIset	Copy Iset from MCH to all members
0	1	0	0	SetVbnds	Copy Vbounds from MCH to all members
0	1	0	1	SetIbnds	Copy Ibounds from MCH to all members
1	0	1	0	SetOn	Switch ON/OFF all members depending on setON in MCH
1	0	1	1	SetEmrgCutOff	Switch OFF all members (Emergeny OFF)
1	1	1	1	Cloning	Set all properties of members like MCH properties *(in preparation)*

MCH3	MCH2	MCH1	MCH0	Value	
0	0	0	0	0	1: Channel 0 is MasterChannel MCH
0	0	0	1	1	1: Channel 1 is MasterChannel MCH
...	...	...	...	...	...
1	1	1	1	15	1: Channel 15 ist MasterChannel MCH

4.5.3.2 Status group

Status groups are used to report the status of a single characteristic of all channels simultaneously. No action is foreseen. Therefore within the group following has to be defined :

Members of the group: Each member will be activated in the channel status list **ChStatLst.**

Type of the group: Status group type **TypeStat**

Channel characteristics: Coding of characteristics , which is to be reported.

EDCP frame: OPC ↑

Access	DATA_DIR	DATA_ID	NBR	OFFSET	DATA_3	DATA_2	DATA_1	DATA_0
master group write	0	0x2000	N_x	O_x	**ChStatList**		**TypeStat**	
master group read-	1	0x2000	N_x	O_x				
HV board write access	0	0x2000	N_x	O_x	**ChStatList**		**TypeStat**	

Nx Group number 0 ... 31

O_x Channel member offset 0, 16, 32 … too access up to 255 channels

ChStatLst DATA_2 to DATA_3 ChannelStatusList members 0x1 … 0xffff UI2

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CH15	CH14	CH13	CH12	CHST11	CHST10	CHST9	CHST8	CHST7	CHST6	CHST5	CHST4	CHST3	CHST2	CHST1	CHST0

TypeStat DATA_0 to DATA_1 TypeStatus UI2

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TYPE1	TYPE0	res	res	res	res	res	res	STAT3	STAT2	STAT1	STAT0	res	res	res	res

TYPE1	TYPE0	Value	
0	1	StatusGroupType	Group will be defined as Status group

STAT3	STAT2	STAT1	STAT0	Value	
0	0	1	1	ChkIsOn	check channel Status.isON (is on)
0	1	0	0	ChkIsRamping	check channel Status.isRAMP (is ramping)
0	1	1	0	ChkIsControlledCurrent	check channel Status.isCC (is current control)
0	1	1	1	ChkIsControlledVoltage	check channel Status.isCV (is voltage control)
1	0	1	0	ChkIsCurrentBounds	check channel Status.isCBNDs (is current bounds)
1	0	1	1	ChkIsVoltageBounds	check channel Status.isVBNDs (is voltage bounds)
1	1	0	0	ChkIsExternalInhibit	check channel Status.isEINH (is external inhibit)
1	1	0	1	ChkIsTrip	check channel Status.isTRIP(is trip)
1	1	1	0	ChkIsCurrentLimit	check channel Status.isCLIM (is current limit exceeded)
1	1	1	1	ChkIsVoltageLimit	check channel Status.isVLIM (is voltage limit exceeded)

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4.5.3.3 Monitoring group

Monitoring groups are used to observe a single characteristic of selected channels simultaneously and in case of need take action. Therefore the group has to be defined :

Members of the group: Each member will be activated in the channel monitoring list **ChMonLst.**

Type of the group: Monitoring group type **TypeMon**

Channel characteristics: Coding of characteristics , which is to be monitored.

Control mode: Coding of the control function, i.e. which kind of change in the group-image shall cause a signal.

Activity: Define , which activity has to happen after the event.

EDCP frame: OPC SNMP ↑

Access	DATA_DIR	DATA_ID	NBR	OFFSET	DATA_3	DATA_2	DATA_1	DATA_0
master group write	0	0x2000	N_x	O_x	**ChMonLst**		**TypeMon**	
master group read-	1	0x2000	N_x	O_x				
HV board write access	0	0x2000	N_x	O_x	**ChMonLst**		**TypeMon**	

Nx Group number 0 ... 31

O_x Channel member offset 0, 16, 32 … too access up to 255 channels

ChMonLst DATA_2 to DATA_3 ChannelMonitoringList members 0x1 … 0xffff UI2

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

TypeMon DATA_0 to DATA_1 TypeMonitoring UI2

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TYPE1	TYPE0	ACT1	ACT0	res	res	res	MOD0	MON3	MON2	MON1	MON0	res	res	res	res

TYPE1	TYPE0	Value	
1	0	MonitoringGroupType	Group will be defined as Monitoring group

ACT1	ACT0	Value	
0	0	0	No special action ; EventGroupStatus[grp] will be set
0	1	1	Ramp down of group EventGroupStatus[grp] will be set
1	0	2	Switch OFF of group without ramp; EventGroupStatus[grp] will be set
1	1	3	Switch OFF of module without ramp; EventGroupStatus[grp] will be set

MOD0	Value	
0	0	event will happen if at least one Channel == 0
1	1	event will happen if at least one Channel == 1

MON3	MON 2	MON 1	MON 0	Value	
0	0	1	1	MonitorIsOn	monitor channel Status.isON (is on)
0	1	0	0	MonitorIsRamping	monitor channel Status.isRAMP (is ramping)
0	1	1	0	MonitorIsControlledCurrent	monitor channel Status.isCC (is current control)
0	1	1	1	MonitorIsControlledVoltage	monitor channel Status.isCV (is voltage control)
1	0	1	0	MonitorIsCurrentBounds	monitor channel Status.isCBNDs (is current bounds)
1	0	1	1	MonitorIsVoltageBounds	monitor channel Status.isVBNDs (is voltage bounds)
1	1	0	0	MonitorIsExternalInhibit	monitor channel Status.isEINH (is external inhibit)
1	1	0	1	MonitorIsTrip	monitor channel Status.isTRIP (is trip)
1	1	1	0	MonitorIsCurrentLimit	monitor channel Status.isCLIM (is current limit exceeded)
1	1	1	1	MonitorIsVoltageLimit	monitor channel Status.isVLIM (is voltage limit exceeded)

4.5.3.4 Delayed Trip group

Trip timeout groups are necessary to keep the timing for the time controlled delayed Trip function and to define the action which has to happen after a Trip.

Therefore in the group following will be defined:

- Members of group: Each member will be activated in a word channel trip timeout list **ChTrpTotLst.**
- Type of the group: Time out group type **TypeTime**
- Activity: Define , which activity has to happen after time controlled Trip
- Timeout: Coding of Timeout-time as integer value.

Timeout groups have to stay unchanged for the whole time as long they are used.
An overwriting will cause the definition of a new group. An overlay of the channels of multiple Trip groups is not allowed.

EDCP frame: OPC SNMP ↑

Access	DATA_DIR	DATA_ID	NBR	OFFSET	DATA_3	DATA_2	DATA_1	DATA_0
master group write	0	0x2000	N_x	O_x	**ChTrpTotLst**		**TypeTime**	
master group read-	1	0x2000	N_x	O_x				
HV board write access	0	0x2000	N_x	O_x	**ChTrpTotLst**		**TypeTime**	

Nx Group number 0 ... 31
O_x Channel member offset 0, 16, 32 … too access up to 255 channels
ChTrpTotLst DATA_2 to DATA_3 ChannelTripTimoutList members 0x1 … 0xffff UI2

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

TypeTime DATA_0 to DATA_1 TypeTimeOut UI2

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TYPE1	TYPE0	ACT1	ACT0	TOT11	TOT10	TOT9	TOT8	TOT7	TOT6	TOT5	TOT4	TOT3	TOT2	TOT1	TOT0

TYPE1	TYPE0	Value	
1	1	TimeOutGroupType	Group will be defined as Timeout group

ACT1	ACT0	Action	
0	0	0	No special action; EventGroupStatus[grp] will be set.
0	1	1	Ramp down of group with ramp; EventGroupStatus[grp] will be set
1	0	2	Switch OFF the group without ramp; EventGroupStatus[grp] will be set
1	1	3	Switch OFF the module without ramp; EventGroupStatus[grp] will be set

TOT[11..0]:	Timeout-time in ms (8..4088ms) resolution is 8ms (different values to 8ms resolution will be rounded)

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4.5.3.5 Set voltage of all channels (group write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master write access	0	0x2100	VoltageSetAllChannels			

VoltageSetAllChannels DATA_0 to DATA_3 [V] R4

(see VoltageSet Single access also)

4.5.3.6 Set current (– trip) of all channels (group write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master write access	0	0x2101	CurrentSetAllChannels			

CurrentSetAllChannels DATA_0 to DATA_3 [A] R4

(see CurrentSet Single access also)

4.5.3.7 Set ON / OFF of all channels (group write- / read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master group write	0	0x2200	SetOnOffAllChs			
master group read-	1	0x2200				
HV board write access	0	0x2200	SetOnOffAllChs			

SetOnOffAllChs DATA_0 to DATA_3 for channel 0 to 31 (channel 16 to 31 are reserved at the moment) UI4

SetOnOffAllChs DATA_2 to DATA_3 for channel 16 to channel 31 (reserved at the moment) UI2

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16

SetOnOffAllChs DATA_0 to DATA_1 for channel 0 to channel 15 UI2

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

$CH_m = 1$ Channel ON

$CH_m = 0$ Channel OFF

The SetOnOffAllChs represents a 32 bit field to control the channel property setON for each channel member of the bit field with one bit in the bit-field. The data point is one of the EDCP group functions with advantage to setON for all channel members simultaneously with on instruction.

4.5.3.8 Set EMERGENCY of all channels (group write- / read-write access)

EDCP frame: ↑

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master group write	0	0x2201	**SetEmergencyAllChs**			
master group read-	1	0x2201				
HV board write access	0	0x2201	**SetEmergencyAllChs**			

SetEmergencyAllChs DATA_0 to DATA_3 for channel 0 to 31 (channel 16 to 31 are reserved at the moment) UI4

SetEmergencyAllChs DATA_2 to DATA_3 for channel 16 to channel 31 (reserved at the moment) UI2

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16

SetEmergencyAllChs DATA_0 to DATA_1 for channel 0 to channel 15 UI2

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

CH_m = 1 Channel EMERGENCY set

CH_m = 0 Channel EMERGENCY reset

The SetEmergencyAllChs represents a 32 bit field to control the channel property setEMCY for each channel member of the bit field with one bit in the bit-field. The data point is one of the EDCP group functions with advantage to setEMCY for all channel members simultaneously with on instruction.

4.5.3.9 Event status voltage limit of all channels (group write- / read-write access)

EDCP frame: ↑

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master group write	0	0x2202	**EventStatusVLimitAllChs**			
master group read-	1	0x2202				
HV board write access	0	0x2202	**EventStatusVLimitAllChs**			

EventStatusVLimitAllChs DATA_0 to DATA_3 for channel 0 to 31 (channel 16 to 31 are reserved at the moment) UI4

EventStatusVLimitAllChs DATA_2 to DATA_3 for channel 16 to channel 31 (reserved at the moment) UI2

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16

EventStatusVLimitAllChs DATA_0 to DATA_1 for channel 0 to channel 15 UI2

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

CH_m = 1 Channel event status voltage limit
CH_m = 0 nothing

The **EventStatusVLimitAllChs** represents a 32 bit field to control the channel property EVLIM for each channel with one bit in the bit-field. The data point is one of the EDCP group functions with advantage to reset EVLIM for all channel members simultaneously with on instruction.

If the voltage limit was exceeded or an external over voltage occurs at the channel output (i.e. Output voltage > Set voltage) then the channel will be switched off and the according bit will be set. The error bits will be canceled and the voltage of the corresponding channel can be switched on again only after writing 'EventStatusVLimitAllChs' with the bits, which are corresponding to the channel errors are set to "1".

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4.5.3.10 Event status current limit of all channels (group write- / read-write access)

EDCP frame: ↑

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master group write	0	0x2203	**EventStatusCLimitAllChs**			
master group read-	1	0x2203				
HV board write access	0	0x2203	**EventStatusCLimitAllChs**			

EventStatusCLimitAllChs DATA_0 to DATA_3 for channel 0 to 31 (channel 16 to 31 are reserved at the moment) UI4

EventStatusCLimitAllChs DATA_2 to DATA_3 for channel 16 to channel 31 (reserved at the moment) UI2

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16

EventStatusCLimitAllChs DATA_0 to DATA_1 for channel 0 to channel 15 UI2

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

$CH_m = 1$ Channel event status current limit
$CH_m = 0$ notihing

The **EventStatusCLimitAllChs** represents a 32 bit field to control the channel property ECLIM for each channel with one bit in the bit-field. The data point is one of the EDCP group functions with advantage to reset ECLIM for all channel members simultaneously with on instruction.

The module responds to the exceeding of the hardware current limit which has been set in the channel in dependence on the according setKILena bit of module control as follows:

setKILena = 1: Voltage will be switched off permanently without ramp, green LED on front panel is off until a write of EventStatusCLimitAllChs with the bits, which are corresponding to the channel errors set to “1”. The error bits will be cancelled and the voltage of the corresponding channels can be switched on again.

setKILena = 0: HV modules without a current control E16D0, E16D1 and E08B0 will be switched off voltage without ramp, green LED on front panel is off. If the output voltage arrives at 0 V the ramping to set voltage will be started automatically again. The green LED again flash only after writing the EventStatusCLimitAllChs with the respective bits.

HV modules with a current control will be not switched off voltage, green LED on front panel is off. The output current will be limited. The green LED flashes only after writing of EventStatusCLimitAllChs with the respective bits and removing of the limitation of current before.

4.5.3.11 Event status trip of all channels (group write- / read-write access)

EDCP frame: ↑

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master group write	0	0x2204	**EventStatusTrpAllChs**			
master group read-	1	0x2204				
HV board write access	0	0x2204	**EventStatusTrpAllChs**			

EventStatusTrpAllChs DATA_0 to DATA_3 for channel 0 to 31 (channel 16 to 31 are reserved at the moment) UI4

EventStatusTrpAllChs DATA_2 to DATA_3 for channel 16 to channel 31 (reserved at the moment) UI2

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16

EventStatusTrpAllChs DATA_0 to DATA_1 for channel 0 to channel 15 UI2

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

$CH_m = 1$ Channel event status trip
$CH_m = 0$ notihing

The **EventStatusTrpAllChs** represents a 32 bit field to control the channel property ETRP for each channel with one bit in the bit-field. The data point is one of the EDCP group functions with advantage to reset ETRP for all channel members simultaneously with on instruction.

If the output current exceeds the programmed current trip value then the corresponding bits will be set:

setKILena = 1: Voltage will be switched off permanently without ramp, green LED on front panel is off until a write of EventStatusTrpAllChs with the bits, which are corresponding to the channel errors set to “1”. The error bits will be cancelled and the voltage of the corresponding channels can be switched on again.

setKILena = 0: HV will be not switched but the green LED on front panel is off. The output current will be limited if there is a current control. The green LED flashes only after writing of EventStatusTrpAllChs with the respective bits and removing of the limitation of current before.

4.5.3.12 Event status inhibit of all channels (group write- / read-write access)

EDCP frame: ↑

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master group write	0	0x2205	**EventStatusInhAllChs**			
master group read-	1	0x2205				
HV board write access	0	0x2205	**EventStatusInhAllChs**			

EventStatusInhAllChs DATA_0 to DATA_3 for channel 0 to 31 (channel 16 to 31 are reserved at the moment) UI4

EventStatusInhAllChs DATA_2 to DATA_3 for channel 16 to channel 31 (reserved at the moment) UI2

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16

EventStatusInhAllChs DATA_0 to DATA_1 for channel 0 to channel 15 UI2

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

$CH_m = 1$ Channel event status inhibit
$CH_m = 0$ notihing

The **EventStatusInhAllChs** represents a 32 bit field to control the channel property ETRP for each channel with one bit in the bit-field. The data point is one of the EDCP group functions with advantage to reset ETRP for all channel members simultaneously with on instruction.

Voltage will be switched off permanently without ramp, if the INHIBIT is active, the green LED on front panel is off. When the INHIBIT is going back from active to passive state then the INHIBIT flag have to be erased by write of the EventStatusInhAllChs before the voltage can be switched on again. The INHIBIT flags are reset with set of the corresponding channel bit to “1”.

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4.5.3.13 Set ON / OFF channels extender (group write- / read-write access)

EDCP frame: ↑

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master group write	0	0x2280	SetOnOffChsExtender			
master group read-	1	0x2280				
HV board write access	0	0x2280	SetOnOffChsExtender			

SetOnOffAllChs DATA_0 to DATA_3 for channel 0 to 31 (channel 16 to 31 are reserved at the moment) UI4

SetOnOffAllChs DATA_2 to DATA_3 for channel 16 to channel 31 (reserved at the moment) UI2

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
CH63	CH62	CH61	CH60	CH59	CH58	CH57	CH56	CH55	CH54	CH53	CH52	CH51	CH50	CH49	CH48

SetOnOffAllChs DATA_0 to DATA_1 for channel 0 to channel 15 UI2

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CH47	CH46	CH45	CH44	CH43	CH42	CH41	CH40	CH39	CH38	CH37	CH36	CH36	CH34	CH33	CH32

$CH_m = 1$ Channel ON

$CH_m = 0$ Channel OFF

The SetOnOffChsExtender represents a 32 bit field to control the channel property setON for each channel member of the bit field with one bit in the bit-field. The data point is one of the EDCP group functions with advantage to setON for all channel members simultaneously with on instruction.

4.5.3.14 Set EMERGENCY channels extender (group write- / read-write access)

EDCP frame: ↑

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master group write	0	0x2201	**SetEmergencyChsExtender**			
master group read-	1	0x2201				
HV board write access	0	0x2201	**SetEmergencyChsExtender**			

SetEmergencyChsExtender DATA_0 to DATA_3 for channel 0 to 31 (channel 16 to 31 are reserved at the moment) UI4

SetEmergencyChsExtender DATA_2 to DATA_3 for channel 16 to channel 31 (reserved at the moment) UI2

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
CH63	CH62	CH61	CH60	CH59	CH58	CH57	CH56	CH55	CH54	CH53	CH52	CH51	CH50	CH49	CH48

SetEmergencyChsExtender DATA_0 to DATA_1 for channel 0 to channel 15 UI2

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CH47	CH46	CH45	CH44	CH43	CH42	CH41	CH40	CH39	CH38	CH37	CH36	CH36	CH34	CH33	CH32

$CH_m = 1$ Channel EMERGENCY set

$CH_m = 0$ Channel EMERGENCY reset

The SetEmergencyChsExtender represents a 32 bit field to control the channel property setEMCY for each channel member of the bit field with one bit in the bit-field. The data point is one of the EDCP group functions with advantage to setON for all channel members simultaneously with on instruction.

4.5.4 Important DCP Module Accesses

4.5.4.1 General status (group write- / read-write / active access)

DCP frame:

Access	EXT_INSTR	DATA_DIR	DATA_ID	DATA_1	DATA_0
HV board active access	0	0	0xc0	GeneralStatus	Details

GeneralStatus DATA_1 UI1
Details DATA_0 UI1

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Save	KILLena/HwVLnotLow	SPLYTMPgd	AvAd	Stbl	SFLPgd	noRamp	noSumErr	INHB	BordTemp	res	res	VLIM	CLIM	RERR	TRP

Save	Save	save function bit stored permanently the current set values (takes some seconds ca. 10s)
KILLena	KillEnable	kill function bit
HwVLnotLow	HardwareVoltageLimitNotLow	hardware voltage limit is not to low bit, for device class 21 only
SPLYTMPgd	SupplyGoodTemperatureGood	supply good and board temperature good bit
AvAd	AverageAdjust	average and fine adjustment bit
SFLPgd	SaftyLoop	safety loop bit
noRamp	noRamp	flag to display that no voltage is ramping
noSumErr	NoSumError	displays that there has been built a sum error flag by VLIM&ILIM&TRP over all channels
INHB	Inhibit	an external INHIBIT at least one of the channels (device class 25)
BoardTemp	BoardTemperatureGood	board temperature is good
VLIM	VoltageLimit	hardware voltage limit has been exceeded
CLIM	CurrentLimit	hardware current limit has been exceeded
RERR	RegulationError	regulation error, for device class 21 only
TRP	Trip	voltage or current trip
res	reserved	

Save=0 no write access to EEPROM
Save=1 store all set values to EEPROM (time to save ca. 10s)

for device classes 24 and 25 only

KILLena=0 kill function disable
KILLena = 1 kill function enable

HwVLnotLow = 0 HW Vlimit voltage limit is to low, it is not possible to switch on the HV, reset by write with HwVLToLow flag is set to “1”
HwVLnotLow = 1 HW Vlimit in proper range

SPLYTMPgd = 0 supply voltages are out of range or module temperature > 55°C
SPLYTMPgd = 1 supply voltages are in range and module temperature <=55°C

AvAd = 0 fine adjustment and average of voltage, current measurement OFF
AvAd = 1 fine adjustment and average of voltage, currentmeasurement ON

Stbl = 0 all channels are stable with program ADC filter frequency f_N. (ADC conversion time =1/f_N, see ‘Set ADC filter frequency‘, default f_N=50 Hz)
Stbl = 1 at least one channel is ramping Vo or not yet stable after ramping (ramping - with ADC filter frequency f_N=100 Hz)

SFLPgd = 0 safety loop is broken -V_O bas been shut off, reset by a write of the ‘General status’ with sloop flag is set to “1”
SFLPgd = 1 safety loop is closed

noRamp = 0 V_O is ramping in at least one channel
noRamp = 1 no channel is ramping

noSumErr = 0 voltage limit, current limit or trip has been exceeded in at least one of the channels (error)
noSumErr = 1 status channel flags v & c & t = 0 for all channels (no errors)

INHB = 0 no external INHIBIT signal
INHB = 1 external INHIBIT signal

BoardTemp = 0 temperature <= 55°C
BoardTemp = 1 temperature > 55°C

VLIM=0 hardware voltage limit hasn’t been exceeded
VLIM=1 hardware voltage limit has been exceeded

CLIM=0 hardware current limit hasn’t been exceeded
CLIM=1 hardware current limit has been exceeded

RERR=0 hardware current hasn’t been exceeded
RERR=1 voltage has been exceeded

TRP=0 no trip
TRP=1 voltage or current trip

If one of the bits noHwVLtoLow, SPLYTMPgd, SFLPgd, noSumErr in the modul access “General status module” has not been set, the module will send this access as an active error message with higher priority (ID9=0). An additional 2nd data byte offers more information about the NoSumError flag of the first byte.

OPC

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Example of an active error message

access	identifier	length code	DATA_ID	DATA_1	DATA_0
HV board active access	0x180	3	0xc0	0x57	0x01

 TRP=1 noSumErr=0 etc.

4.5.4.2 Log-on / Log-off Front-end device at superior layer (module active- / write access)

DCP frame: OPC ↑

Access	DATA_DIR	DATA_ID	DATA_1	DATA_0
HV board active access	1	0xD8	GeneralStatus	DeviceClass
master write access	0	0xD8	LogOnOff	

GeneralStatus DATA_1 – refer chapter 4. UI1

DeviceClass DATA_0 UI1

device class EDCP	DCP	label	firmware	description	associated serial numbers
21	0	EDS	E16D0_xxx E16D1_xxx E24D1_xxx	EDS 16 channels per PCB EDS 16 channels per PCB EDS 24 channels per PCB	471xxx / 71xxxx
22	-	HPS / LPS	H101C0_5xx	HPS 19”, 1 channel HV Power Supply (300W, 800W)	68xxxx / 70xxxx
23	-	HPS / LPS	H201C0_2xx	HPS compact,1 channel HV Power Supply (350W)	68xxxx / 70xxxx
24	6	EHS/EMS/ELS	E08C0_xxx	ExS 8 channel per PCB, standard common GND	473xxx / 74xxxx
25	7	EHS/EMS/ELS	E08F0_xxx	ExS 8 channel per PCB, standard, floating GND	474xxx
26	2	EHS/EMS/ELS	E08F2_xxx	ExS 8 channel per PCB, floating GND 2 ranges for measurement of current	72xxxx
27	-	EHS/EMS/ELS	E08C2_xxx	ExS 8 channel per PCB, common floating GND 2 ranges for measurement of current	78xxxx
41	-	MICC	MICC_3xx	MICC Multichannel Interface Crate Controller for MMC Crates	458xxx
42	-	MICP	MICP_3xx	MICP Multichannel Interface Crate PHQ Controller for MMC Crates	458xxx
60	-	HPS	H101C1_1xx	HPS 19”, 1 channel HV Power Supply (1.5kW – 10 kW)	90xxxxx
70	-	EHS	E16C1_1xx	ExS 16 channels per PCB or 32 channels per module	79xxxx

LogOnOff DATA_1=1 superior layer send a “Log-on” at Front-end device to registration UI1
DATA_1=0 superior layer send “Log-off” to Front-end device
xxx and xxxx are running numbers

After POWER ON the Front-end device - up to a number of two per module - will give this module access cyclically on the bus (ca. 1 sec). If a controller of superior layer identifies this access then it is possible to register this as a Front-end device and is possible to address it with FE_ADR. (see also description 11bit-Identifier)

After the successful registration the Front-end device will not send further ‘Log-on” accesses as long as:

- it receives accesses from the external CAN Bus in periods shorter than one minute or
- until the superior controller will send a ‘Log-off” access to the Front-end device.

4.5.5 Events

The module provides an extended event collecting logic. This is necessary to monitor extraordinary events and forward them to the host.

4.5.5.1 Channel events

These event-bits in the channel event status register are related to mask bits in the channel event mask register. With help of an AND function (bit-wise) between an event bit and the according mask bit a result only occurs where the mask bit has been set. A following logic OR function of all of these results leads to the event status of the channels.

ModuleEventChannelStatus[ch] =
(ChannelEventStatus.EVLIM[ch] AND ChannelEventMask.MEVLIM[ch]) OR
(ChannelEventStatus.ECLIM[ch] AND ChannelEventMask.MECLIM[ch]) OR
(ChannelEventStatus.ETRP[ch] AND ChannelEventMask.METRP[ch]) OR
(ChannelEventStatus.EEINH[ch] AND ChannelEventMask.MEEINH[ch]) OR
(ChannelEventStatus.EVBNDs[ch] AND ChannelEventMask.MEVBNDs[ch]) OR
(ChannelEventStatus.ECBNDs[ch] AND ChannelEventMask.MECBNDs[ch]) OR
(ChannelEventStatus.ECV[ch] AND ChannelEventMask.MECV[ch]) OR
(ChannelEventStatus.ECC[ch] AND ChannelEventMask.MECC[ch]) OR
(ChannelEventStatus.EEMCY[ch] AND ChannelEventMask.MEEMCY[ch]) OR
(ChannelEventStatus.EEOR[ch] AND ChannelEventMask.MEEOR[ch]) OR
(ChannelEventStatus.EOn2Off[ch] AND ChannelEventMask.MEOn2Off [ch]) OR
(ChannelEventStatus.EIER[ch] AND ChannelEventMask.MEIER[ch])

ch={0..n}

The status of all channel events is collected in the register EventChannelStatus of the module items.
For a selection or filtering of the channel events a related mask register has been provided (ModuleEventChannelMask). With help of the AND or OR function (see channel) the event active signal of the channels EventChannelActive will be generated:

EventChannelActive = (EventChannelStatus[0] AND EventChannelMask[0]) OR
(EventChannelStatus[1] AND EventChannelMask[1]) OR
...
(EventChannelStatus[n] AND EventChannelMask[n])

4.5.5.2 Group events (in preparation)

Like written before groups are also able to generate Events. These events will be collected in the status word EventGroupStatus of the GroupData. With help of the mask register EventGroupMask the event active signal of the groups EventGroupActive will be generated..

EventGroupActive = (EventGroupStatus[0] AND EventGroupMask[0]) OR
(EventGroupStatus[1] AND EventGroupMask[1]) OR
...
(EventGroupStatus[23] AND EventGroupMask[24])

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4.5.5.3 Module events

With help of the NOT, AND or OR function the event active signal of the module EventModuleActive will be generated:

EventModuleActive = (NOT(ModuleEventStatus.ETMPngd) AND ChannelEventMask.METMPngd) OR
(NOT(ModuleEventStatus.ESPLYngd) AND ChannelEventMask.MESPLYngd) OR
(NOT(ModuleEventStatus.ESFLPngd) AND ModuleEventMask.MESFLPngd) OR

From both signals EventChannelActive and EventModuleActive the global event active signal of the module IsEventActive of the ModuleStatus register will be generated.

IsEventActive = EventChannelActive OR EventGroupActive OR EventModuleActive

This global signal 'IsEventActive' triggers a fast message on the CAN bus with the DCP Module frame of General status.

Example:

The event flag ECC of the ChannelEventStatus for channel 2 or the event flag EventTemperatureNotGood of the ModuleEventStatus should release a fast CAN frame:

- Channel[2].ChannelEventMask.Bit.MECC = 1
- Module.EventChannelMask.Bit.2 = 1

- Module.EventMask.Bit.METMPngd = 1

The signal isEvntActive is triggerd and release a fast CAN frame of General status when:

(Channel[2].ChannelEventStatus.Bit.ECC & Channel[2].ChannelEventMask.Bit.MECC &
Module.ModuleEventChannelMask.Bit2

OR

Module.ModuleEventStatus.Bit.ETMPngd & Module.ModuleEventMask.Bit.METMPngd

(Module.ModuleEventChannelStatus.Bit2 & Module.ModuleEventChannelMask.Bit2)

Fast CAN frame in case of Channel[2].ChannelEventStatus.Bit.ECC == 1:

0x190 3 0xc0 0x3700 (ID=0x190, ID9=0; Len=3; DATA_ID=0xc0; Data=0x3700)

(Channel[2].ChannelEventStatus.Bit.ECC & Channel[2].ChannelEventMask.Bit.MECC)==1 ➡ ModuleEventChannelStatus.Bit2=1

Fast CAN frame in case of Module.ModuleEventStatus.Bit. ETMPngd == 1:

0x190 3 0xc0 0x1740 (ID=0x190, ID9=0; Len=3; DATA_ID=0xc0; Data= 0x1740)

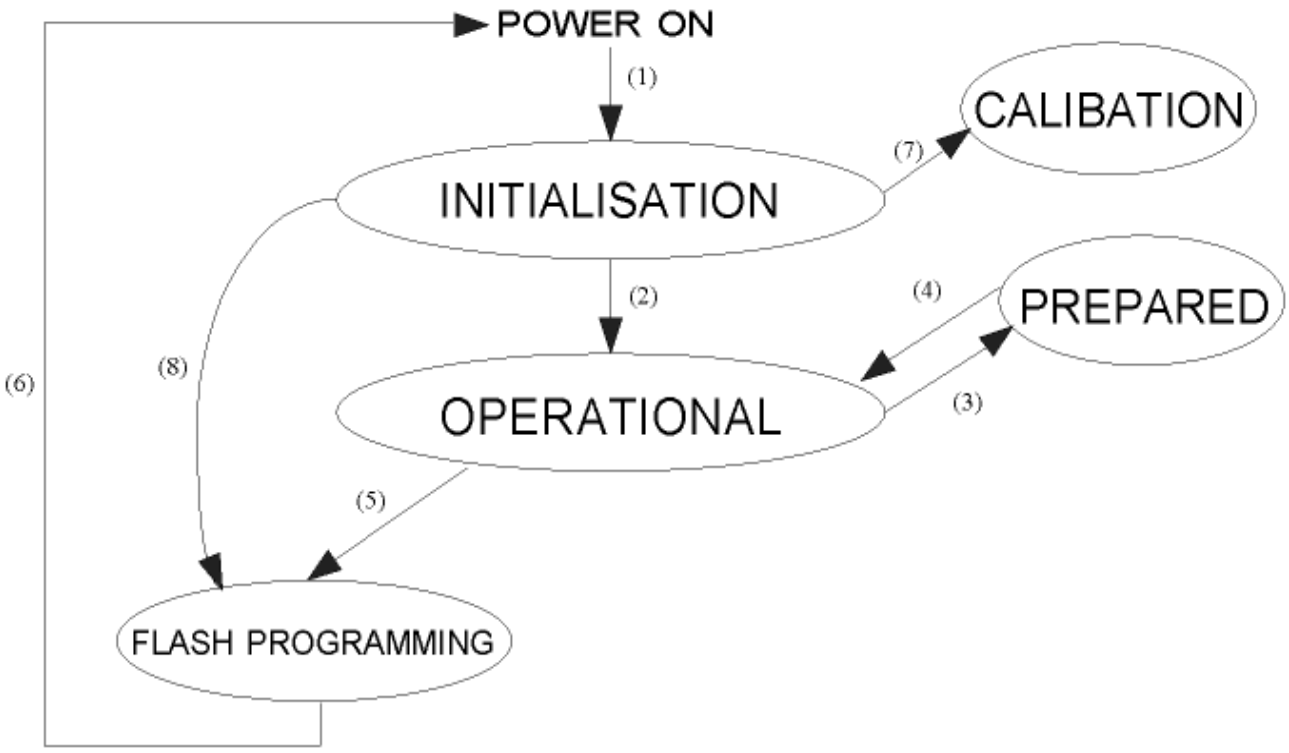
Please note that, a release of a fast CAN frame is different in handling depending on EDCP or DCP mode!

Appendix A – Shortcuts

BCD	binary coded decimal format
CAN	controller area network
Ch_m	channel m=0..15
CHN	channel
DCP	device control protocol
DATA_ID	data identifier of DCP
f_N	first filter notch frequency
HV	High voltage
HW	hardware
I_{meas}	Actual current
I_{max}	Hardware current limit
$I_{O\ max}$	Nominal current
I_{set}	Set current
I_{trip}	Trip current
ISO	International Standard Organization
LSB	least significant bit
MBR	channel members
MSB	most significant bit
NBR	group number
NMT	network management service
OSI	Open System Interconnect
PCB	printed circuit board
p/a	passive / active
SN.	serial number
UI1	unsigned character
SI1	signed character
UI2	unsigned short integer (16 bit)
UI3	unsigned integer (24 bit)
UI4	unsigned integer (32 bit)
R4	float according to IEEE-754 single precision format
V_{meas}	Actual voltage
V_{max}	Hardware voltage limit
$V_{O\ max}$	Nominal voltage
V_{set}	Set voltage
SW	software

Jumper for the safety-loop on the rear side

Appendix B – Diagram of operating modes



(1) The INITIALIZATION follows after the POWER ON reset of the device hardware. It can be differ between different device classes.

(2) The state OPERATIONAL will be obtained by the device itself if all initializations are ready or the state PREPARED runs in time out.

(3) NMT Stop switches the devices of the CAN segment into the state PREPARED. In this state the permanent settings of the devices can be changed (per device *Bit rate, Set voltage, Set current, Ramp speed, General status, Threshold to arm the errors detection, Discharge relay configuration, CAN message configuration* and additional the *Bit rate* as a broadcast massage).

(4) NMT Start takes the devices of the CAN segment back to the OPERATIONAL state.

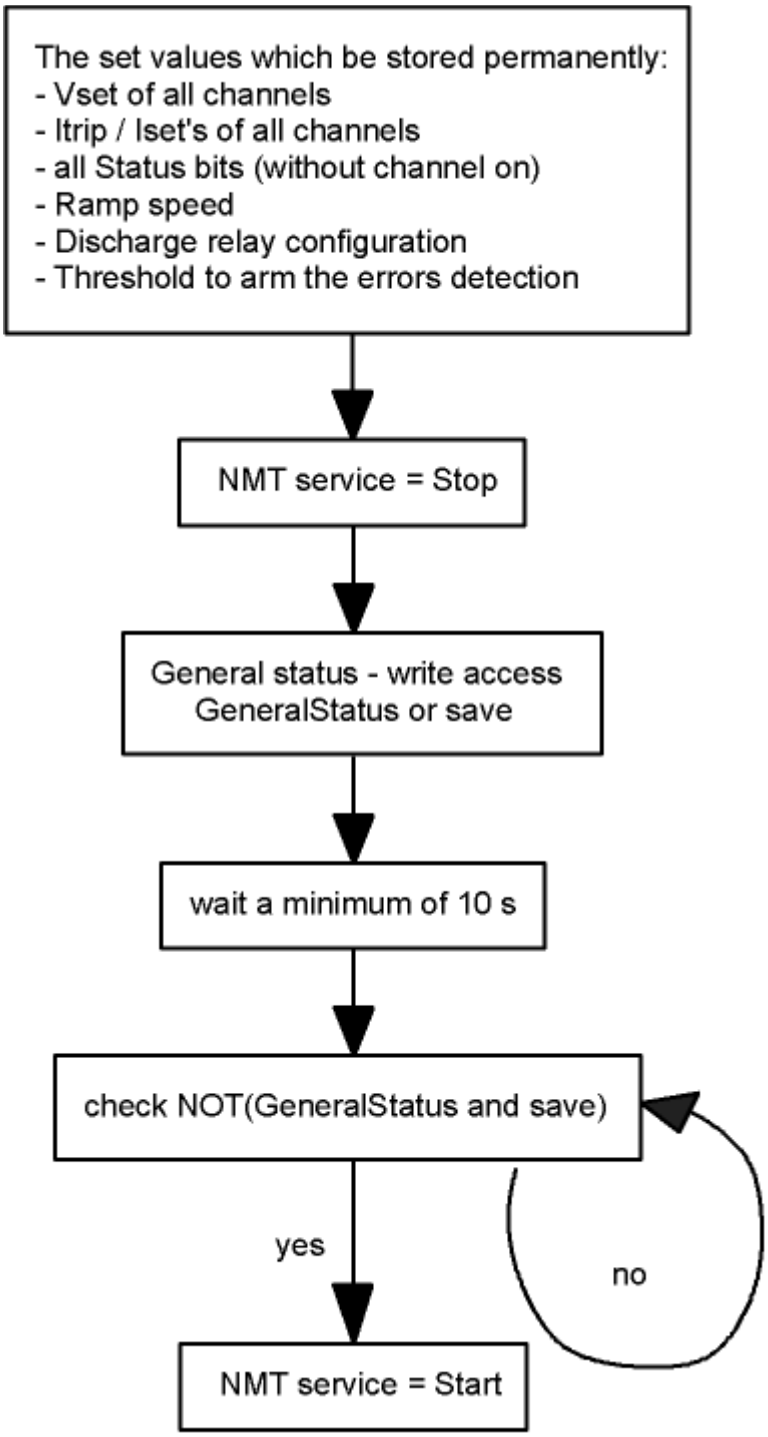
(5) With the special *Flash programming* access the device runs into the state FLASH PROGRAMMING. The high voltage will be switched off automatically before.

(6) The device will execute a POWER ON reset itself at the end of FLASH PROGRAMMING.

(7) The state CALIBRATION will be obtained by setting of the corresponding switches at the Calibration Crate.

(8) The state FLASH Programming will be obtained also if the corresponding switch at the Calibration Crate / Flash Programming Slot are set.

Appendix C – Programming flowchart to store the settings permanently with help of General state save bit



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Appendix D – Programming flowchart to store the configurations of the module permanently with help of General state save bit